

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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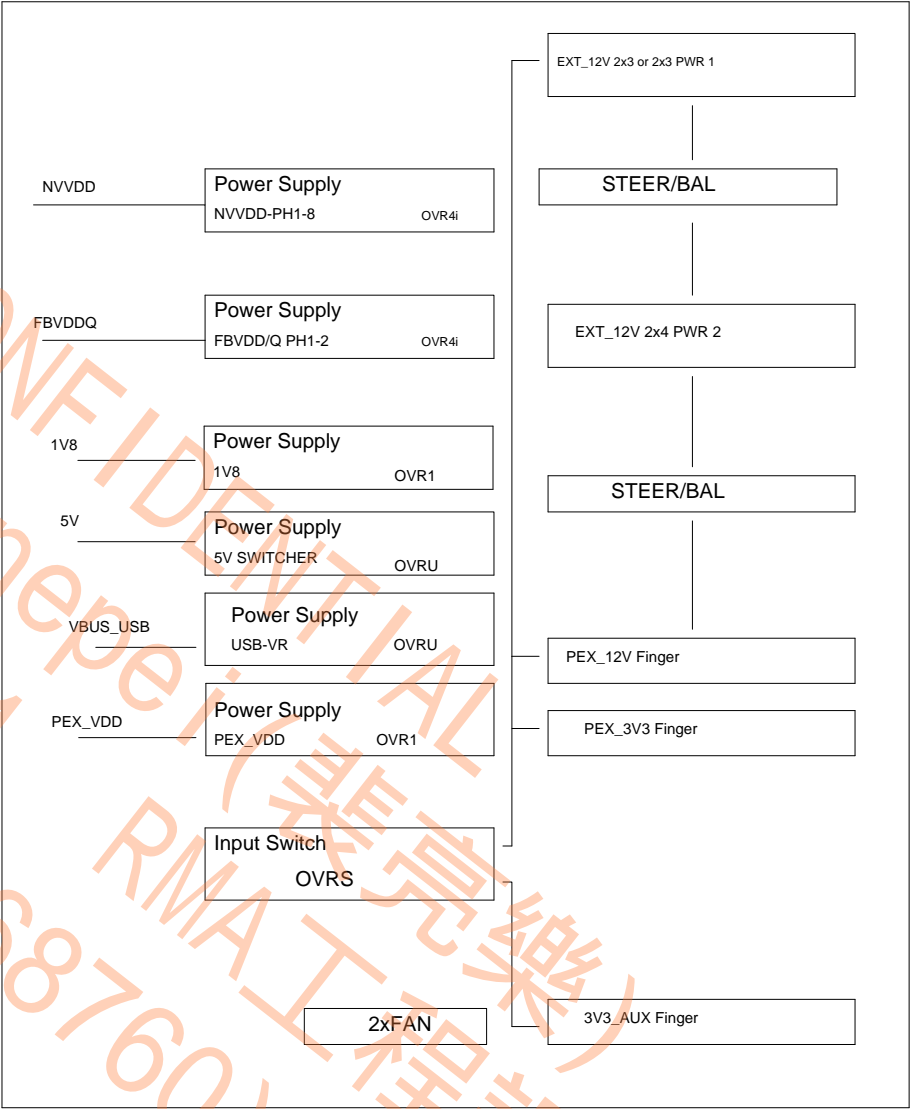
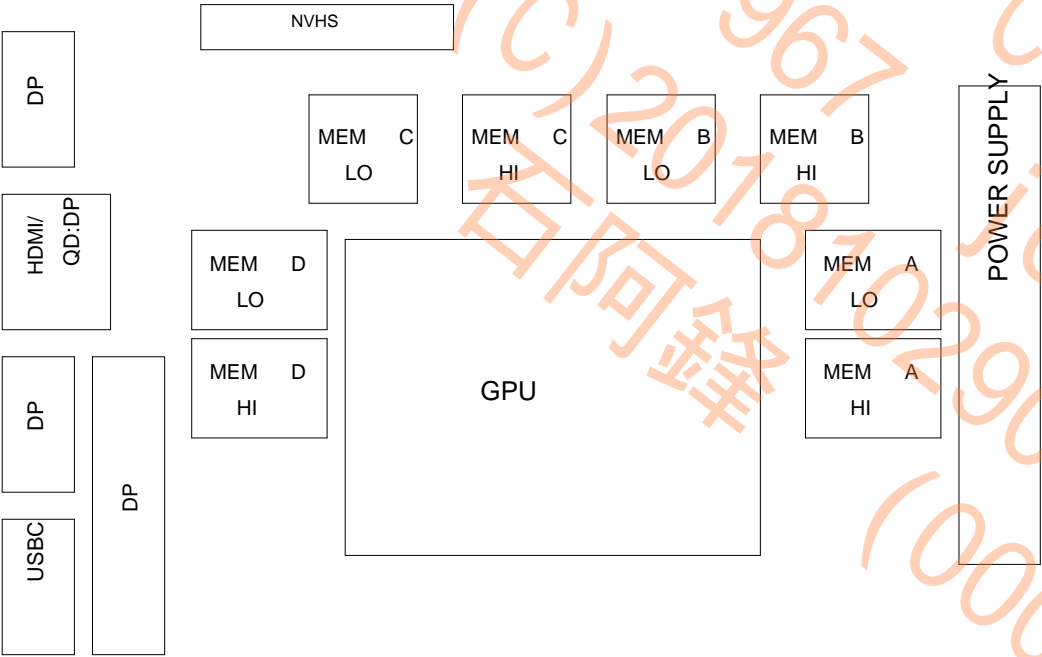
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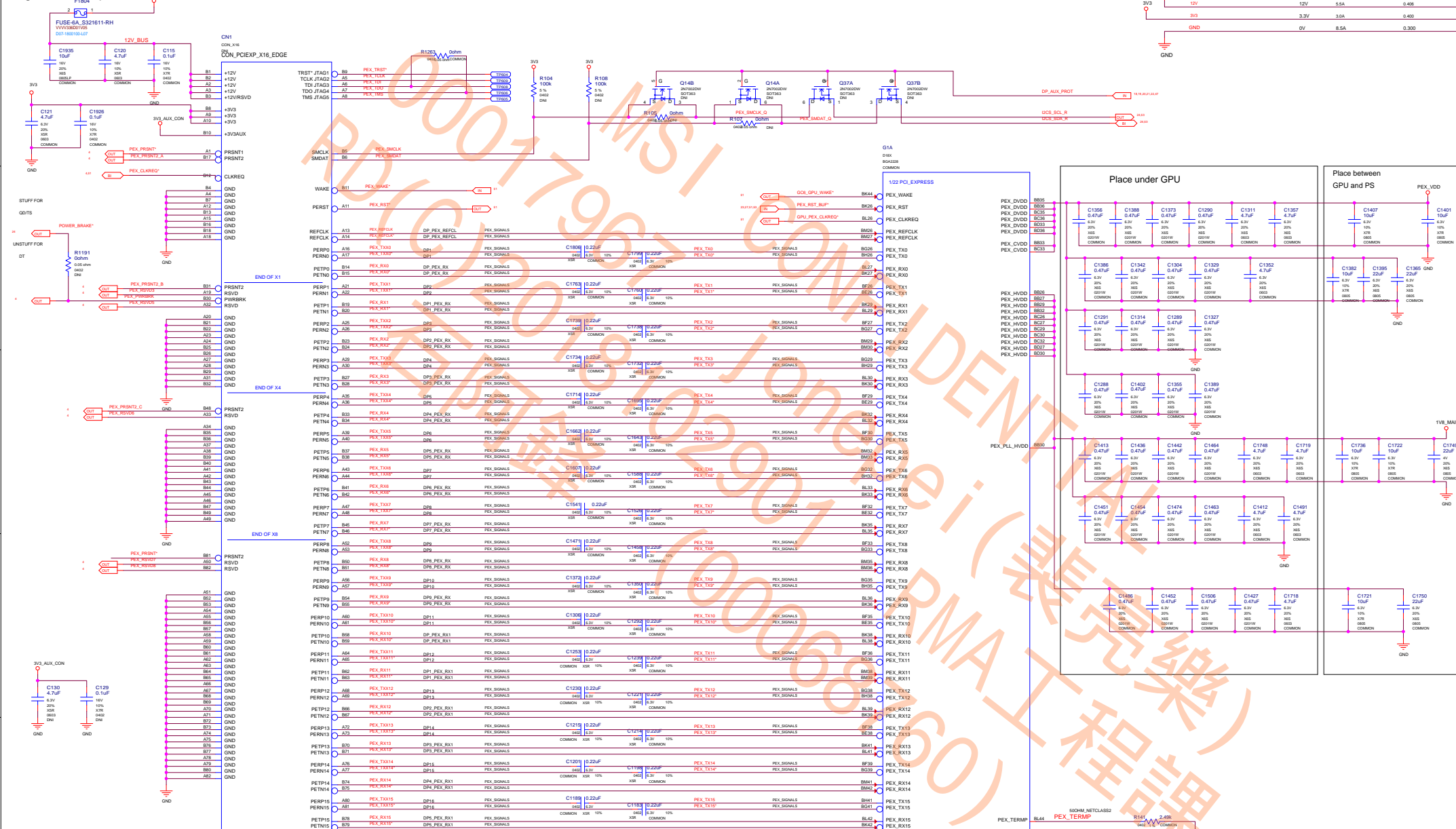
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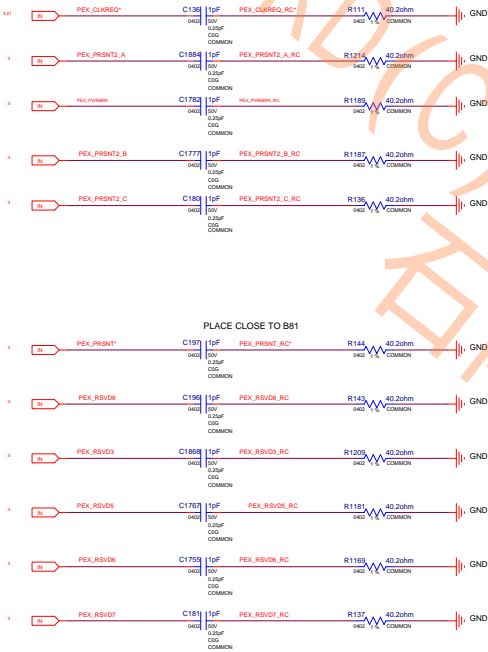
51	SEQUENCE: MISC
52	LED & FAN HEADERS
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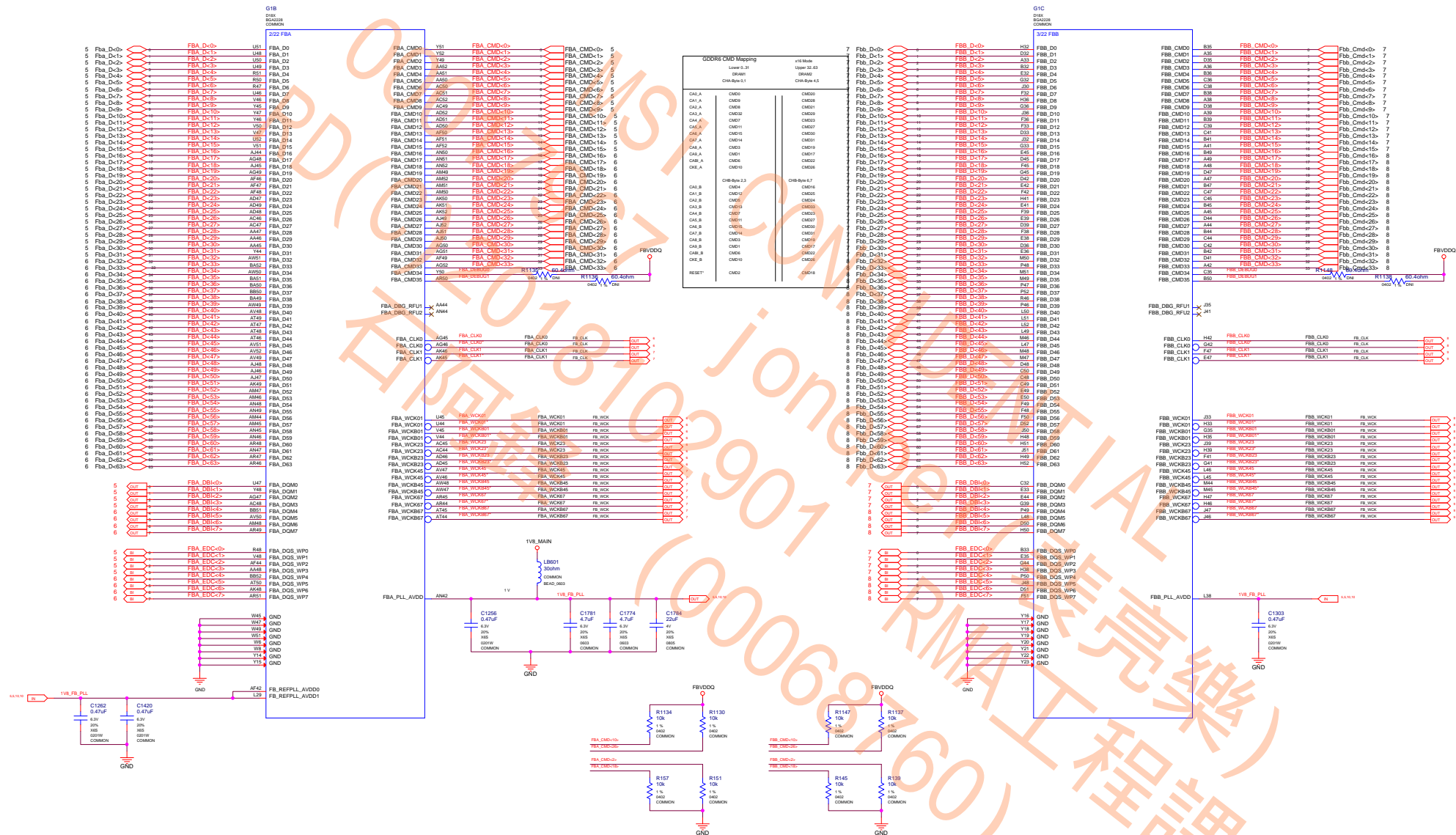
base on V372-02S change for D18 Z
 1. P.23 remove SL1 & BRIDGE_LED_VDD & SL1_BRG_PRST*
 2. P.52 remove LED change FAN connector
 3. P.53 remove LED
 4. P.38/44 add FUSE
 5. P.5~14 mem add <>
 6. P.53 LED use V336-0D
 7. P.32 remove
 8. P.35~38 dual MOS
 9. P.33 change dual MOS
 10. P.43 remove
 11. P.31 change to UP1666
 12. P.21 remove colay DP



VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	5.5A	0.406
3.3V	3.0A	0.400
0V	8.5A	0.300



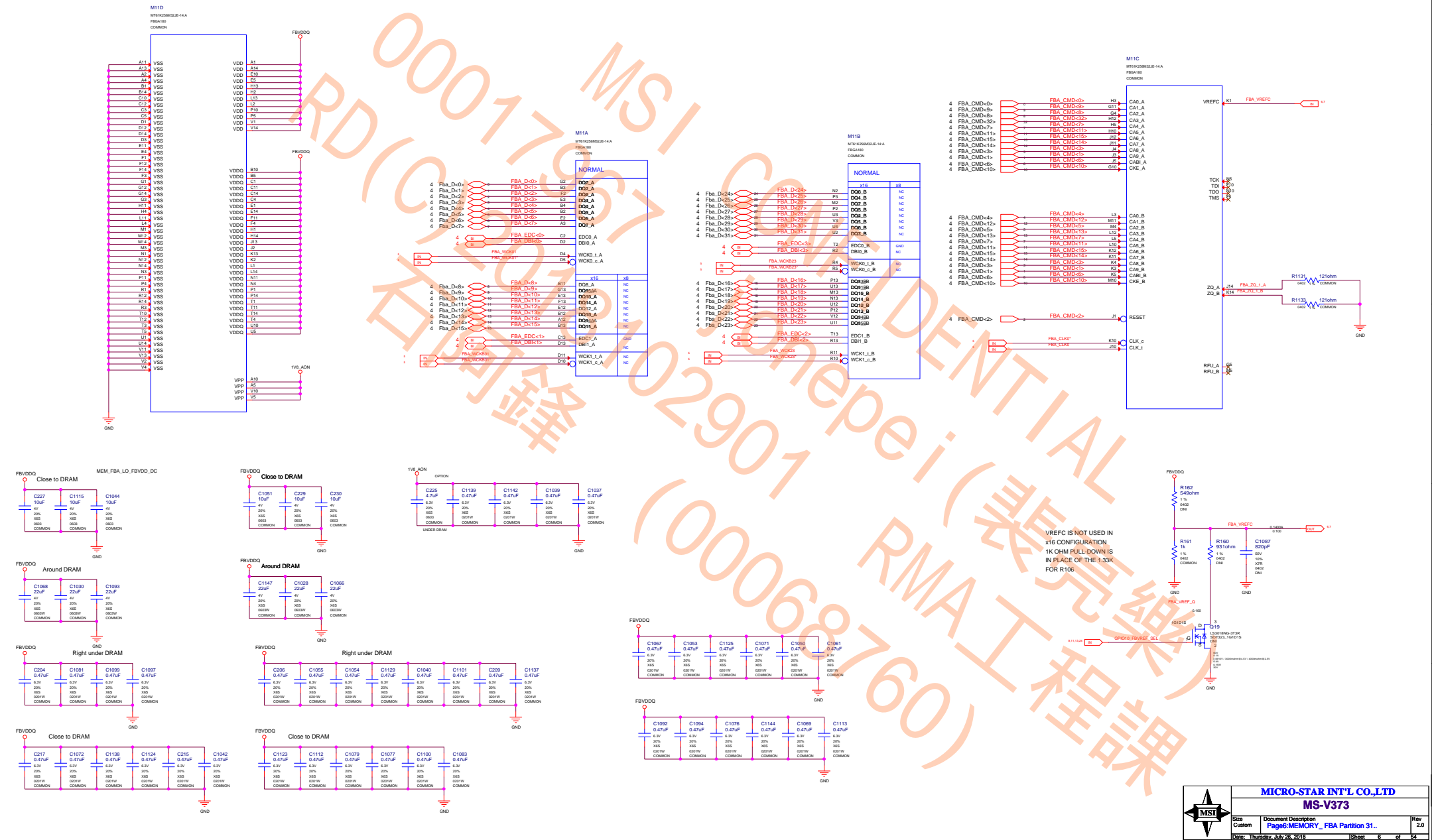


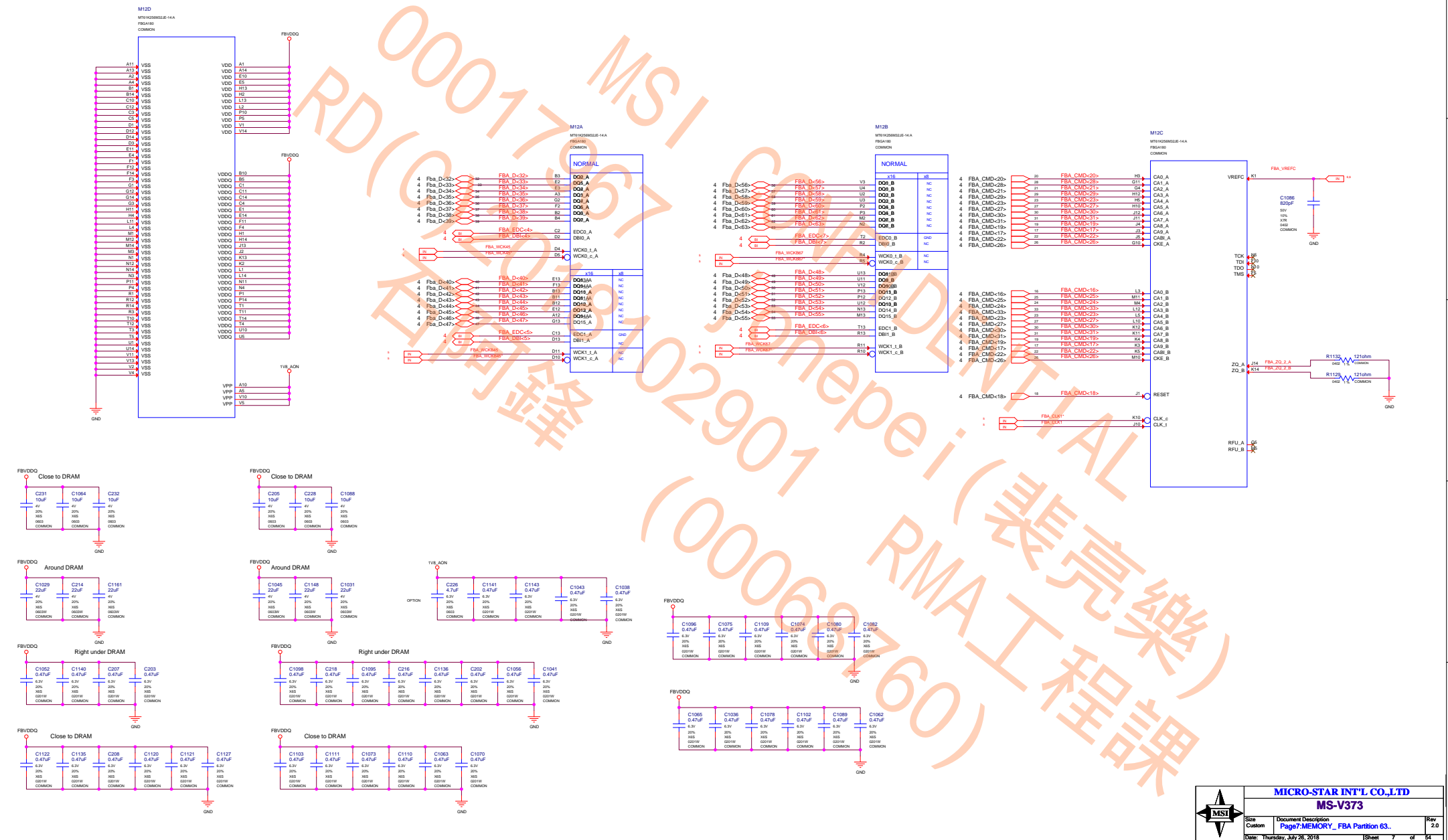


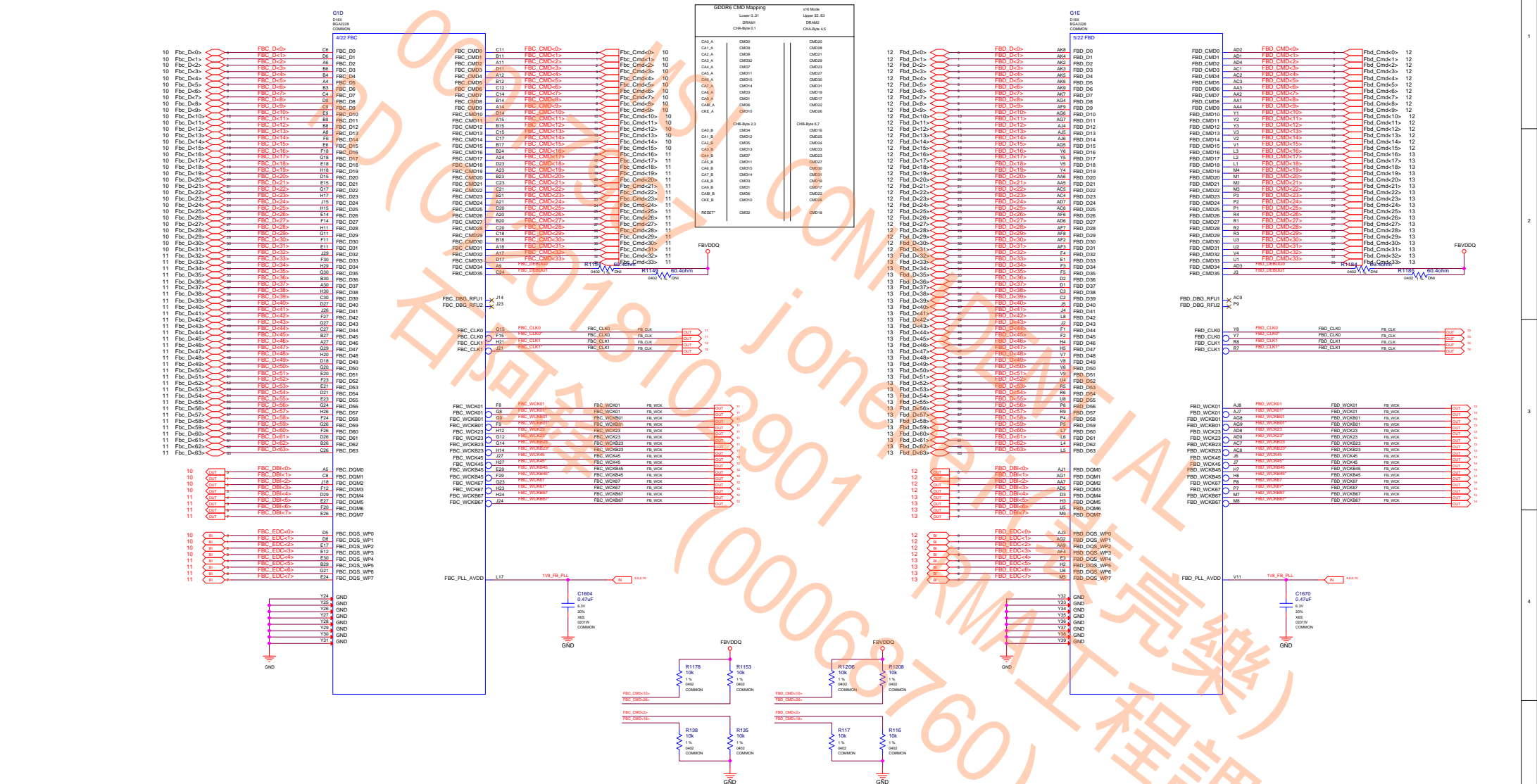
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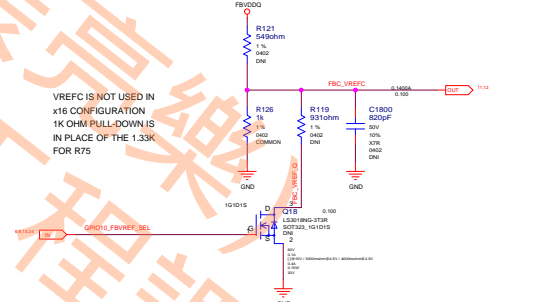
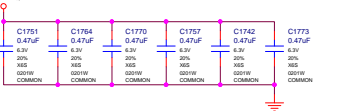
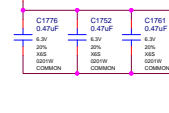
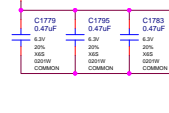
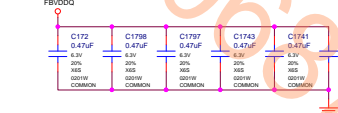
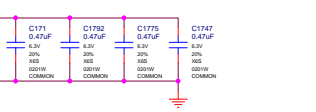
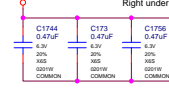
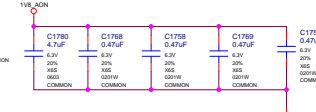
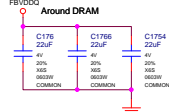
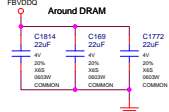
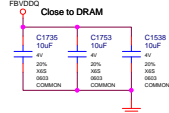
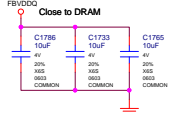
MS-V373

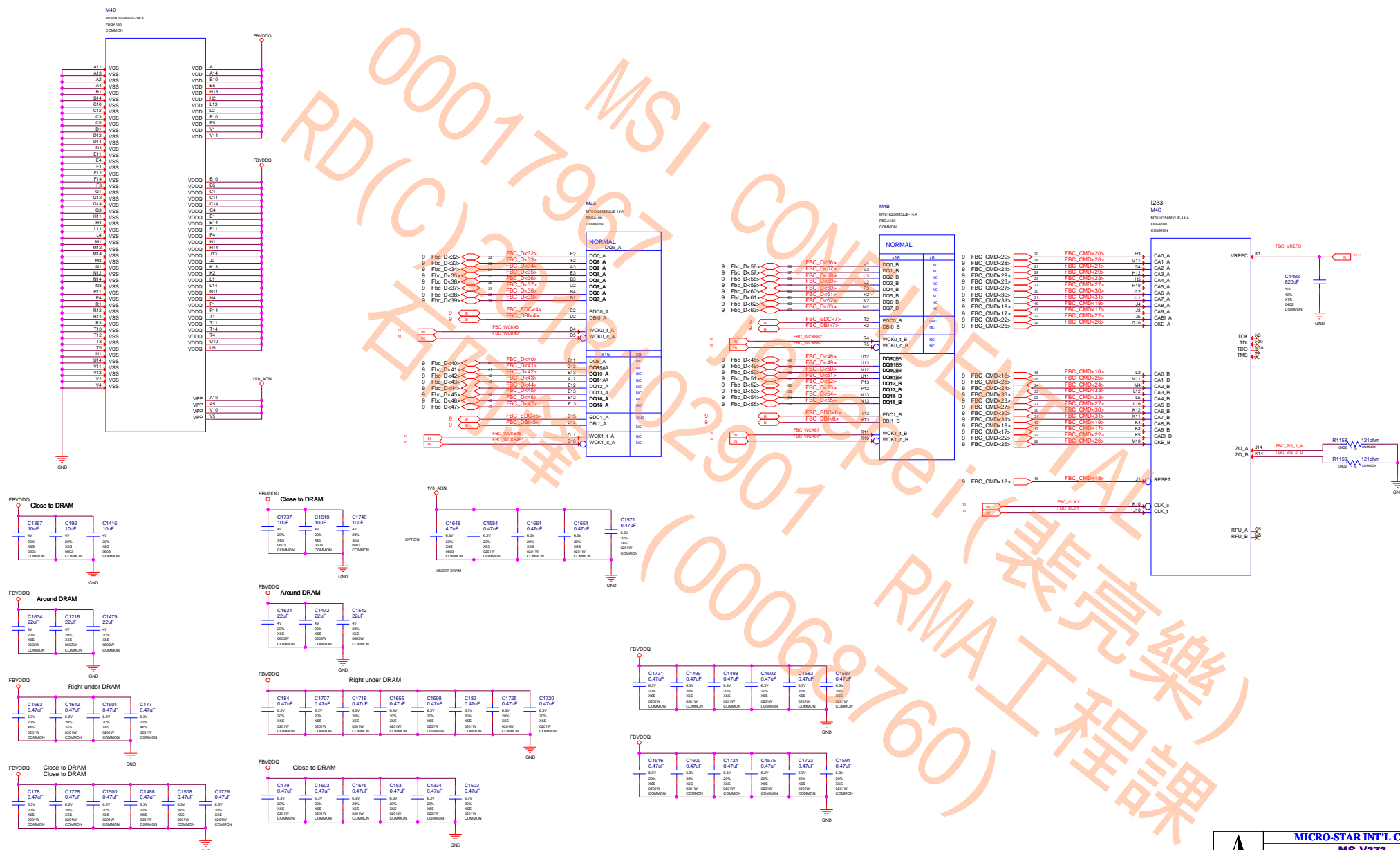
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Custom	Page5:MEMORY_GPU Partition A_B	2.0
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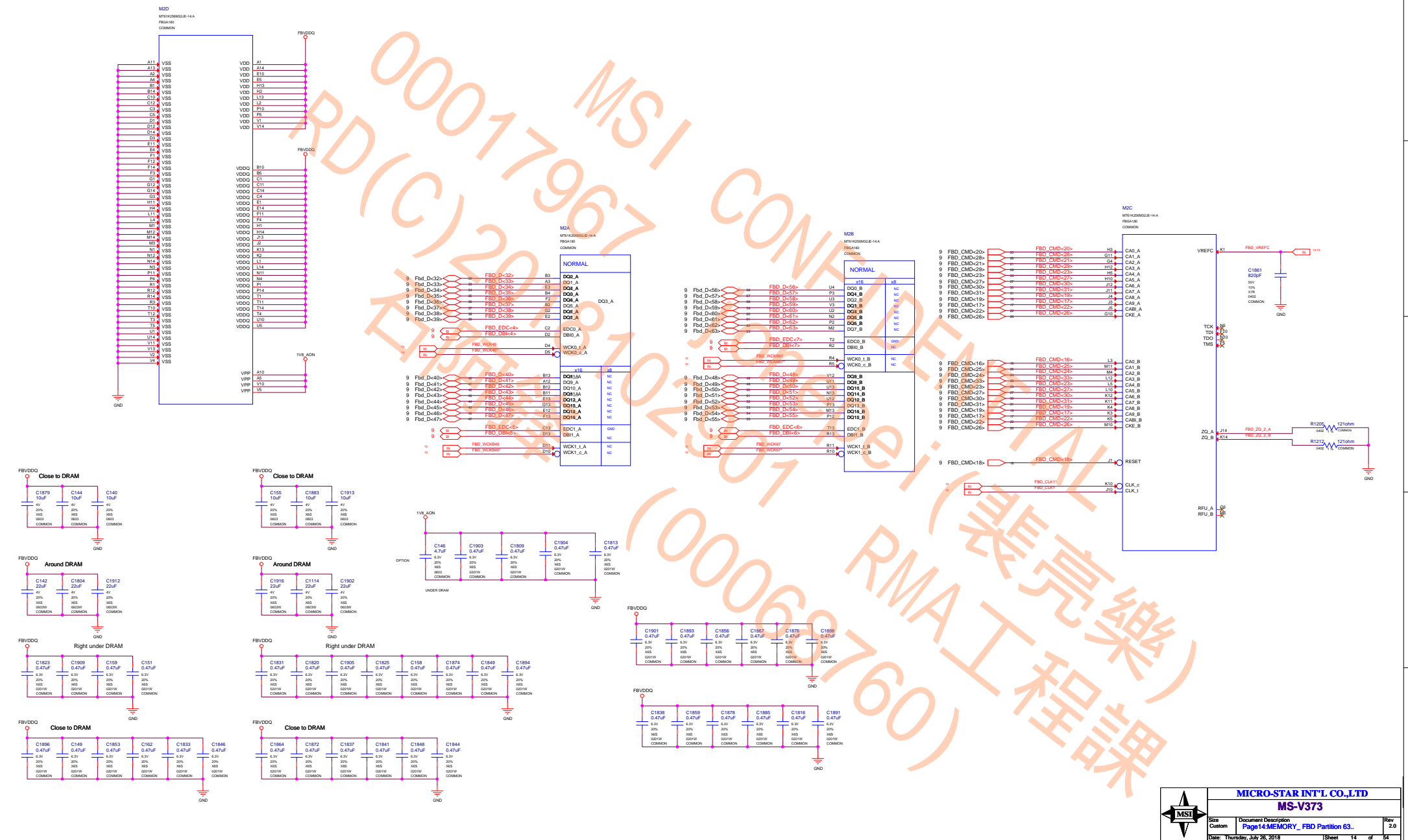


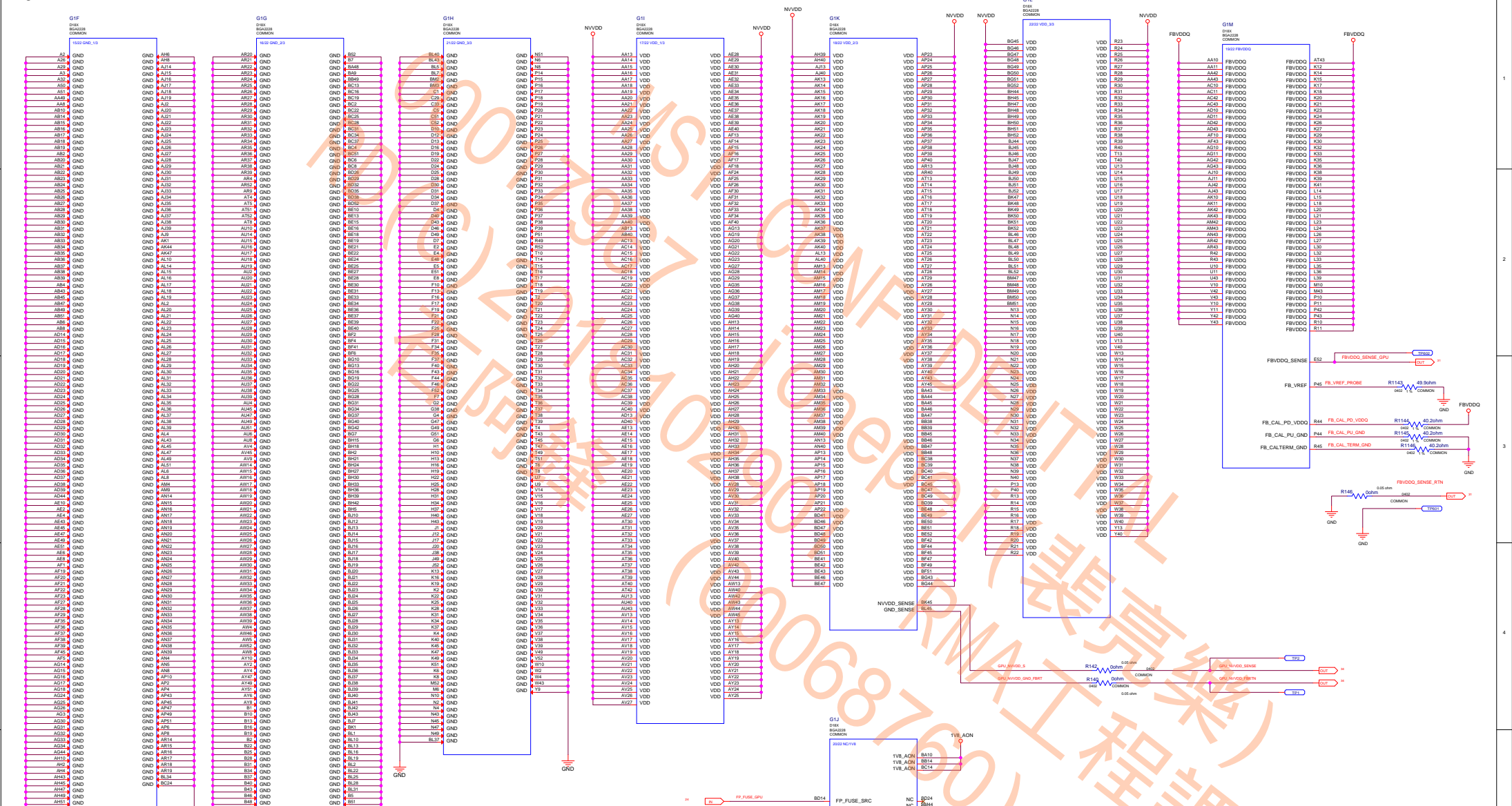










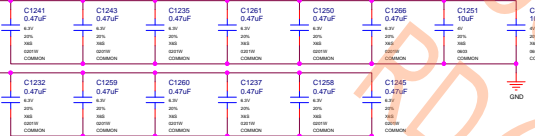


NVVDD

FBVDDQ

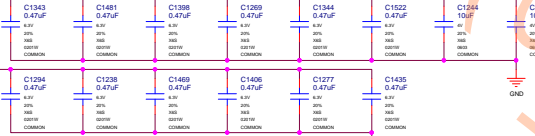
Partition A

6x 1uF and 2x 10uF



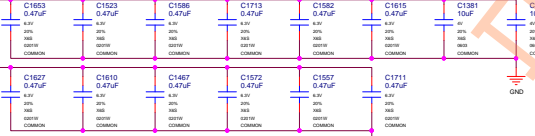
Partition B

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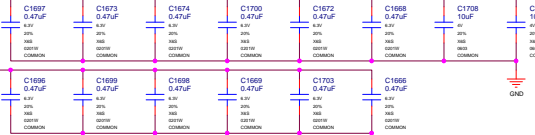
Partition C

6x 1uF and 2x 10uF



Partition D

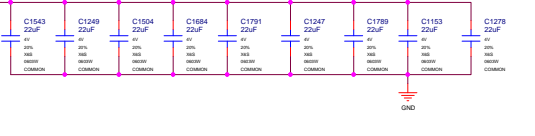
6x 1uF and 2x 10uF



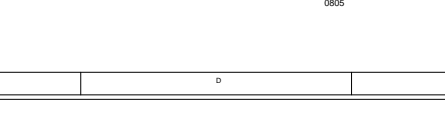
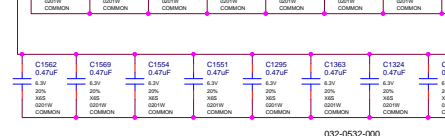
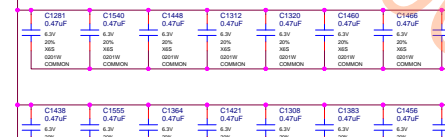
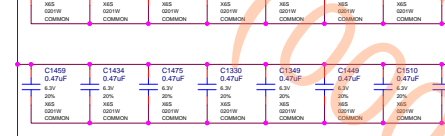
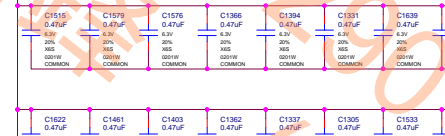
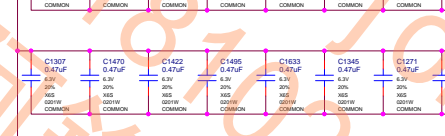
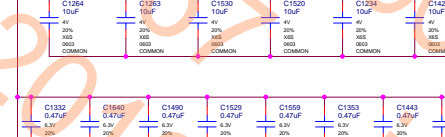
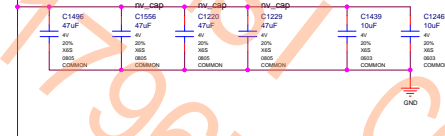
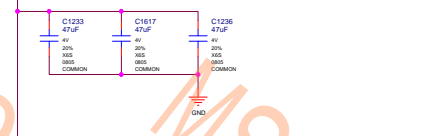
Place Close to GPU



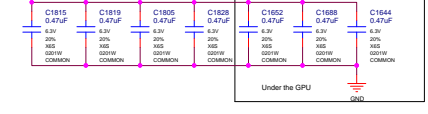
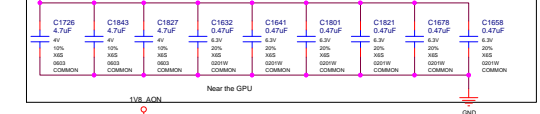
Place Close to GPU



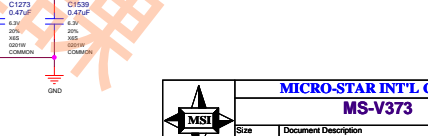
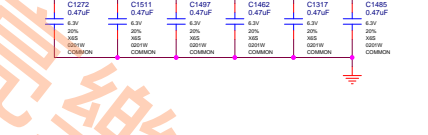
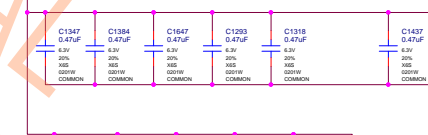
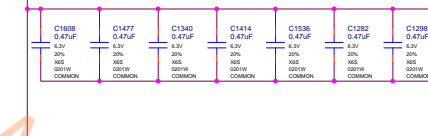
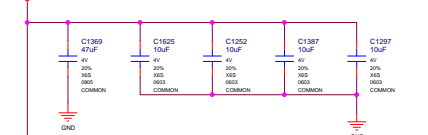
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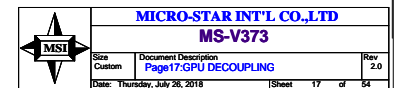
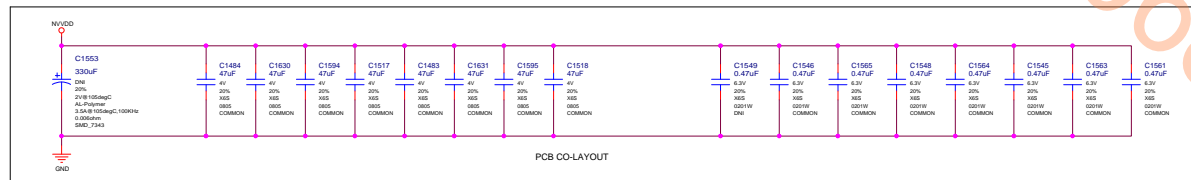
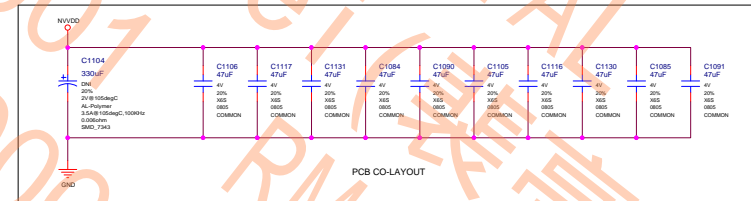
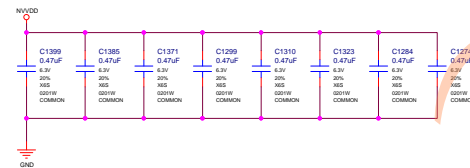
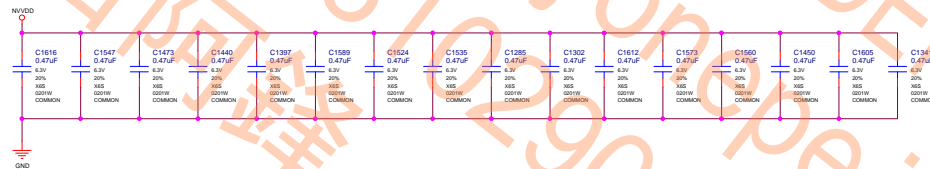
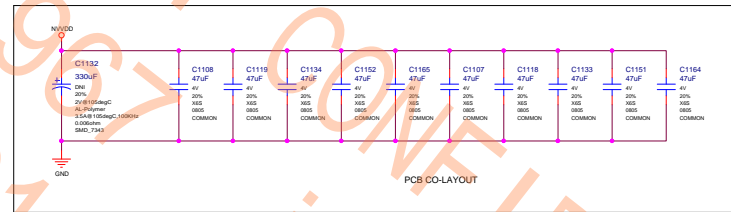
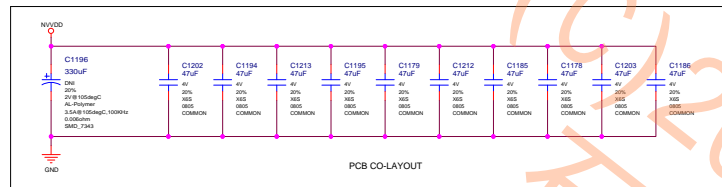
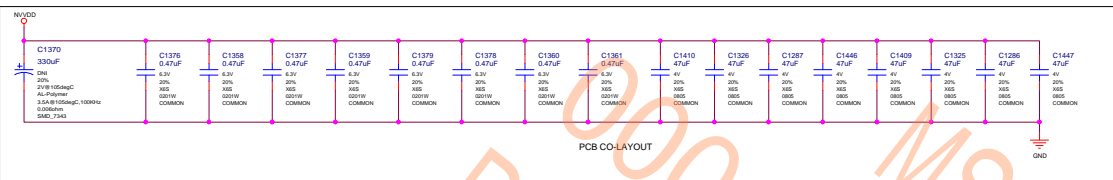
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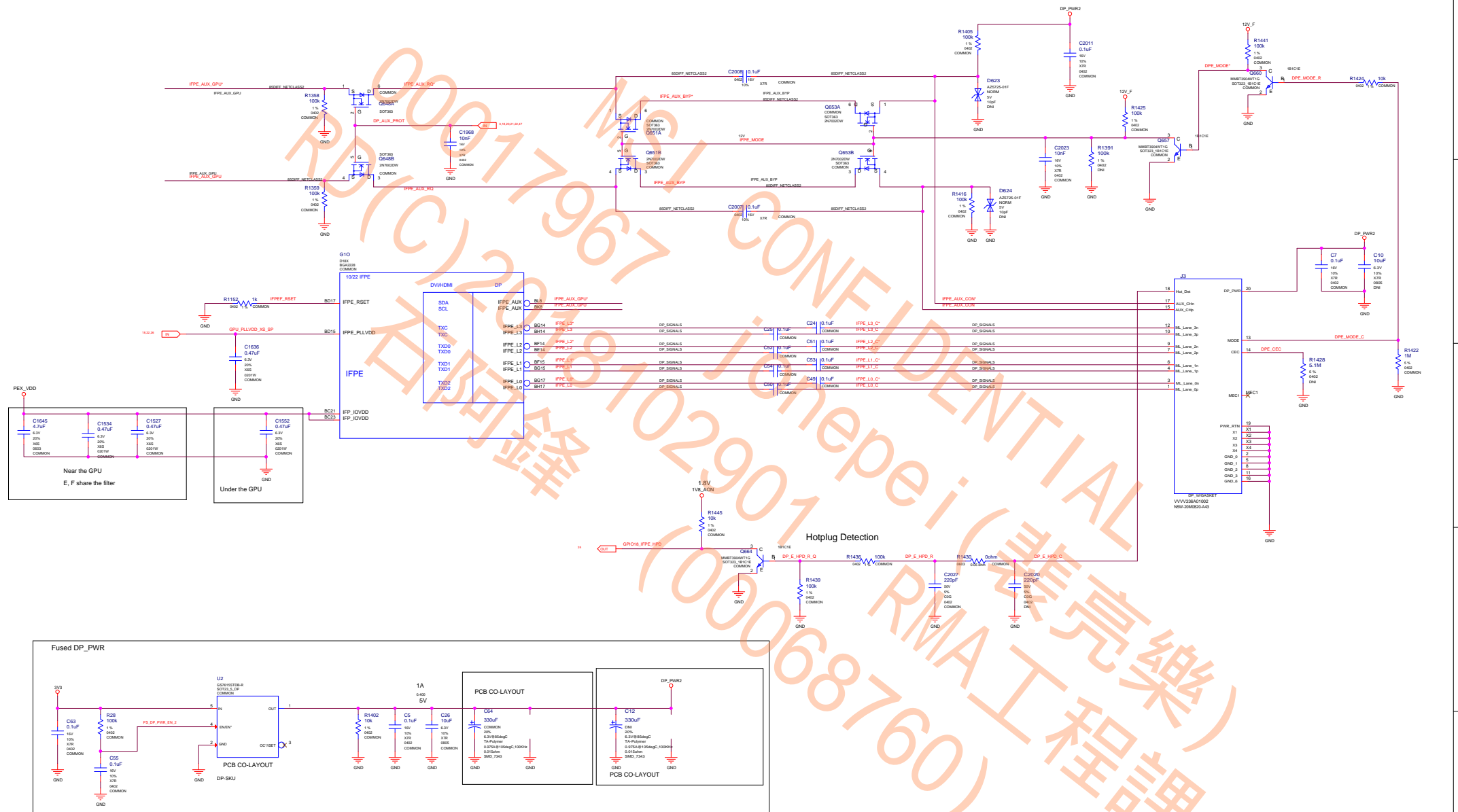
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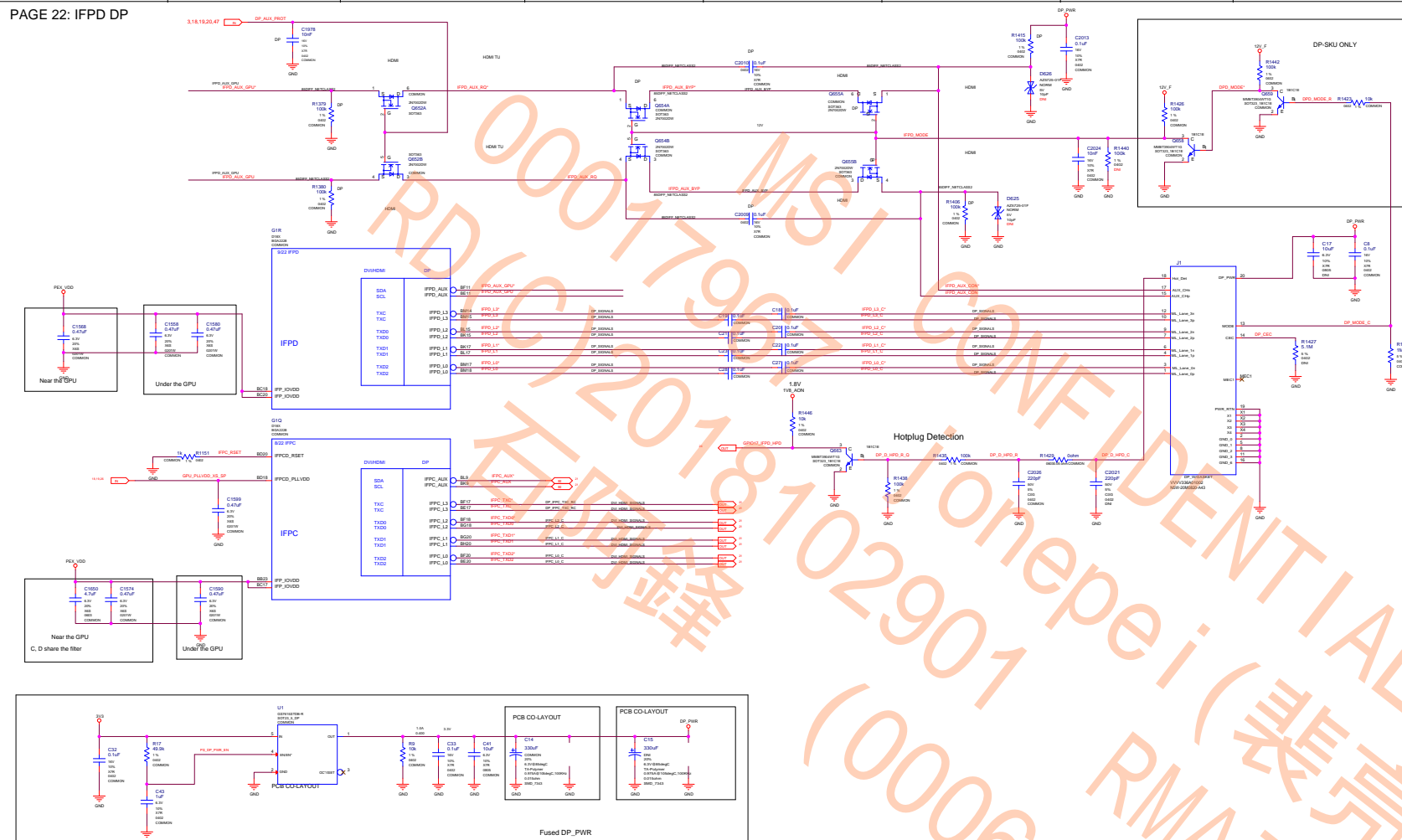


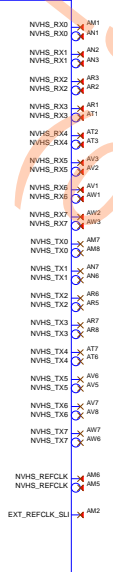
NVVDD


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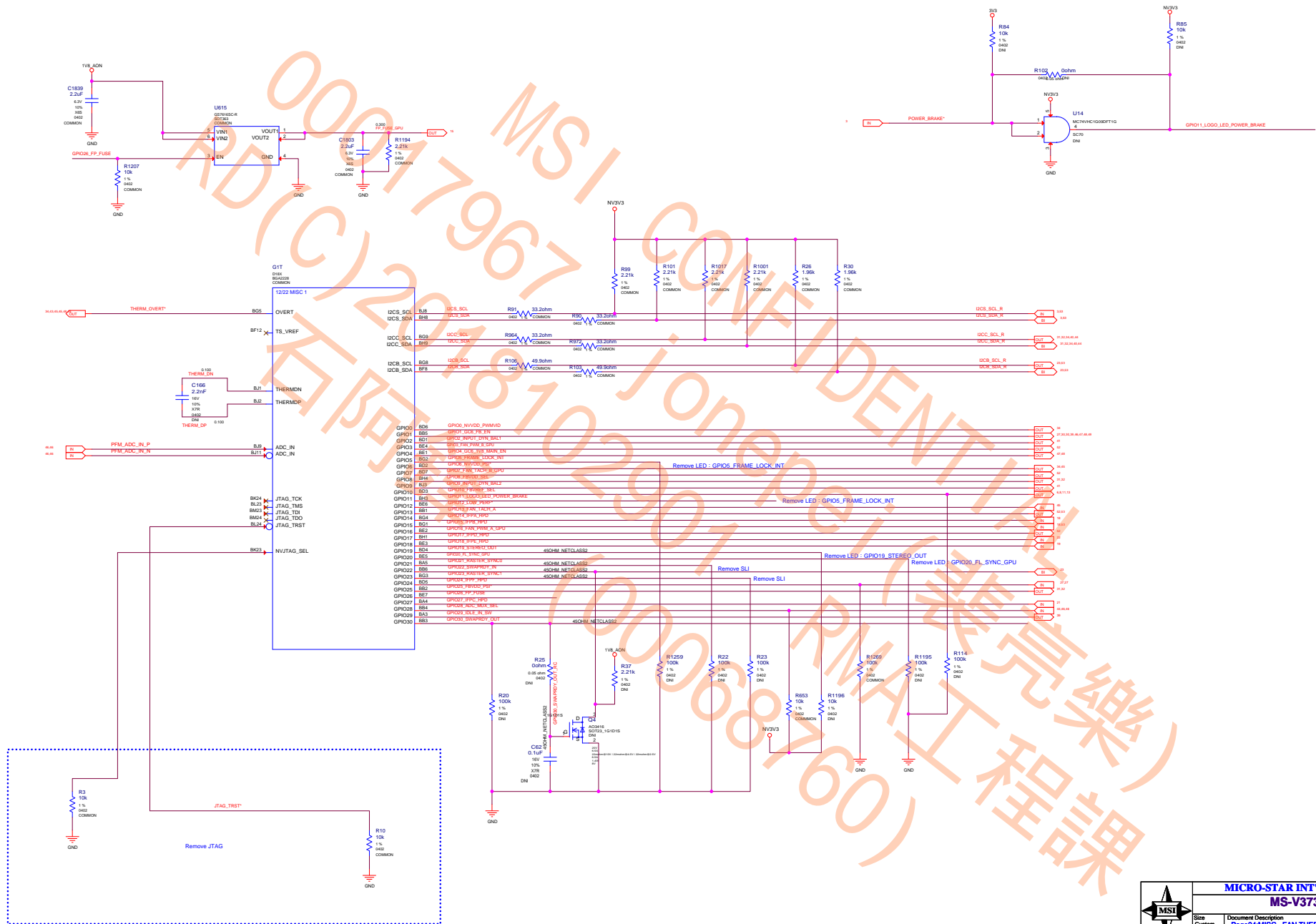








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H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]_FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

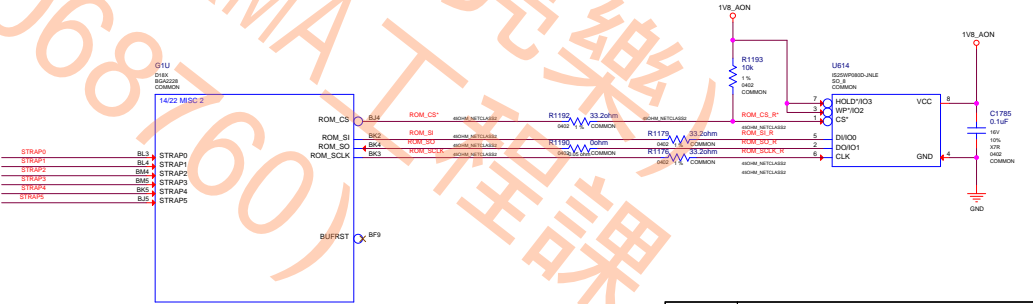
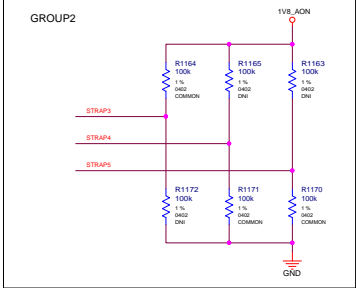
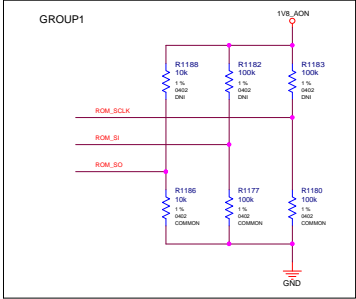
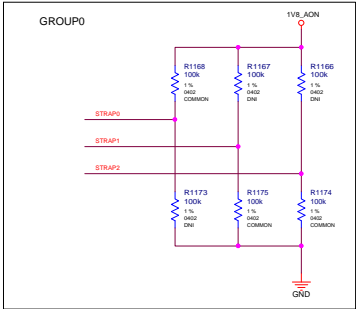
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

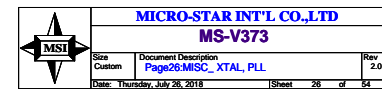
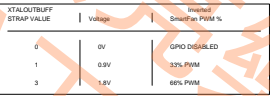
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

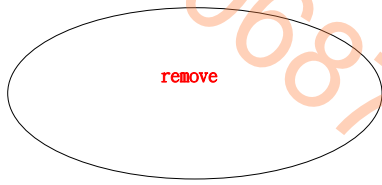
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

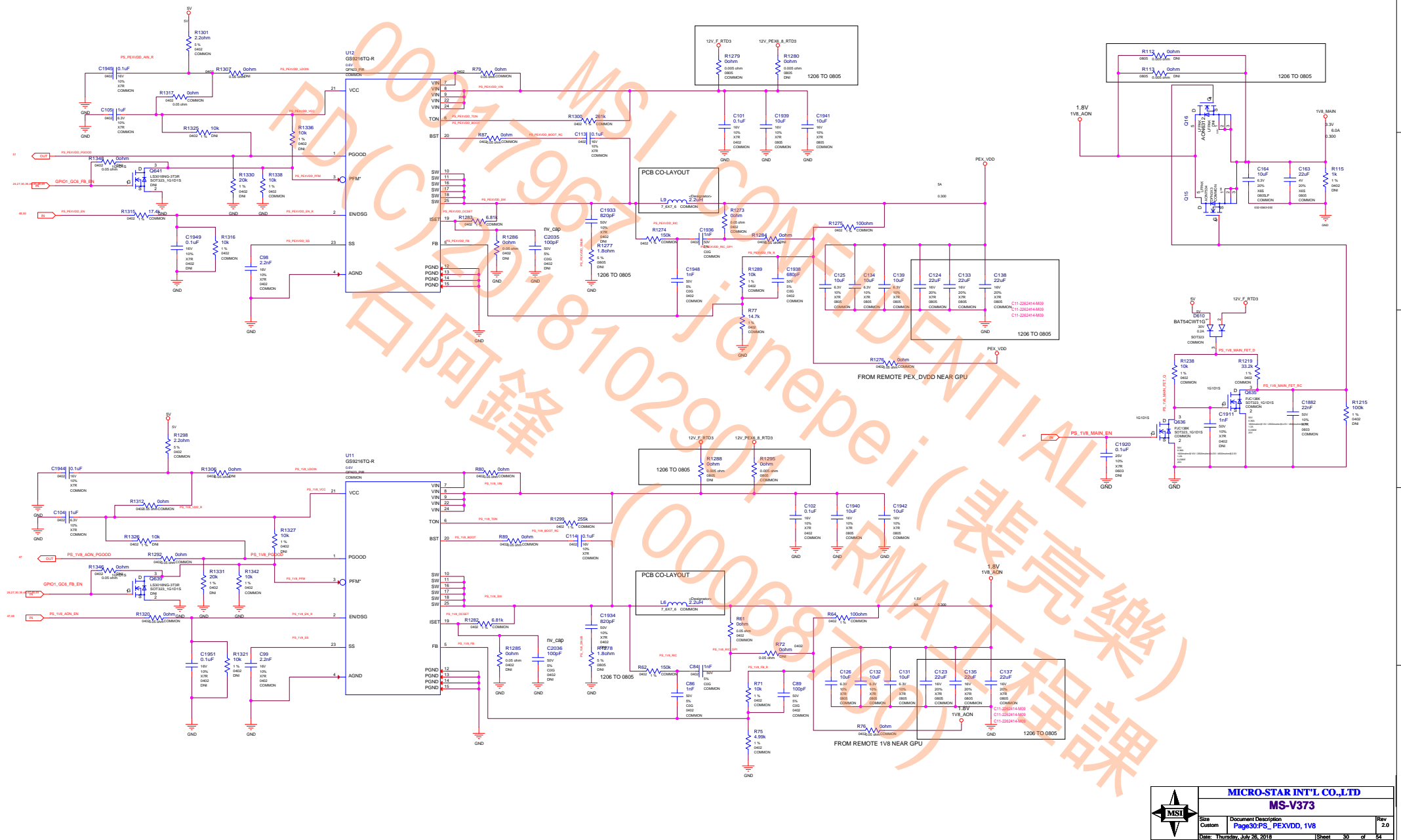
Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung




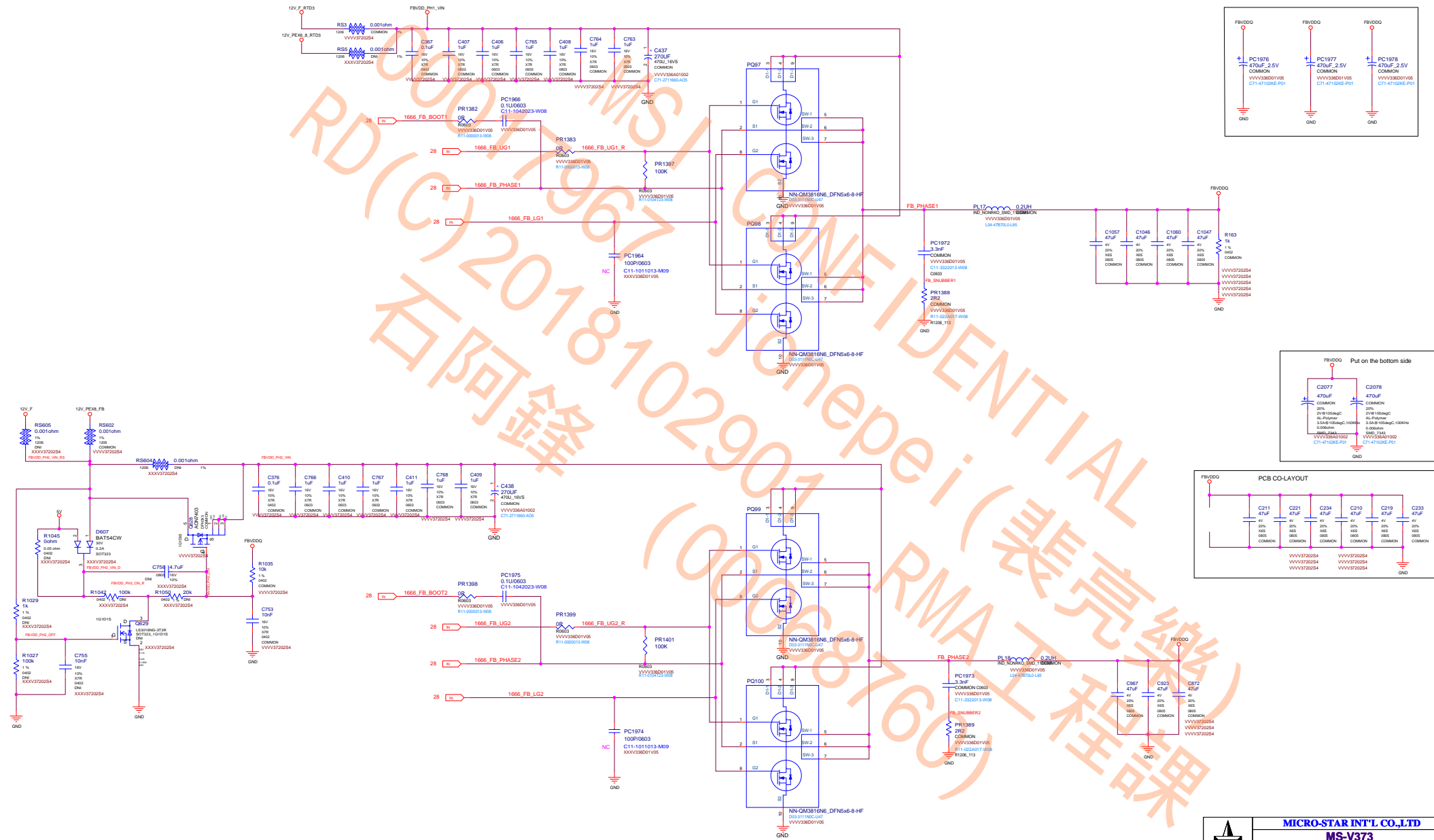


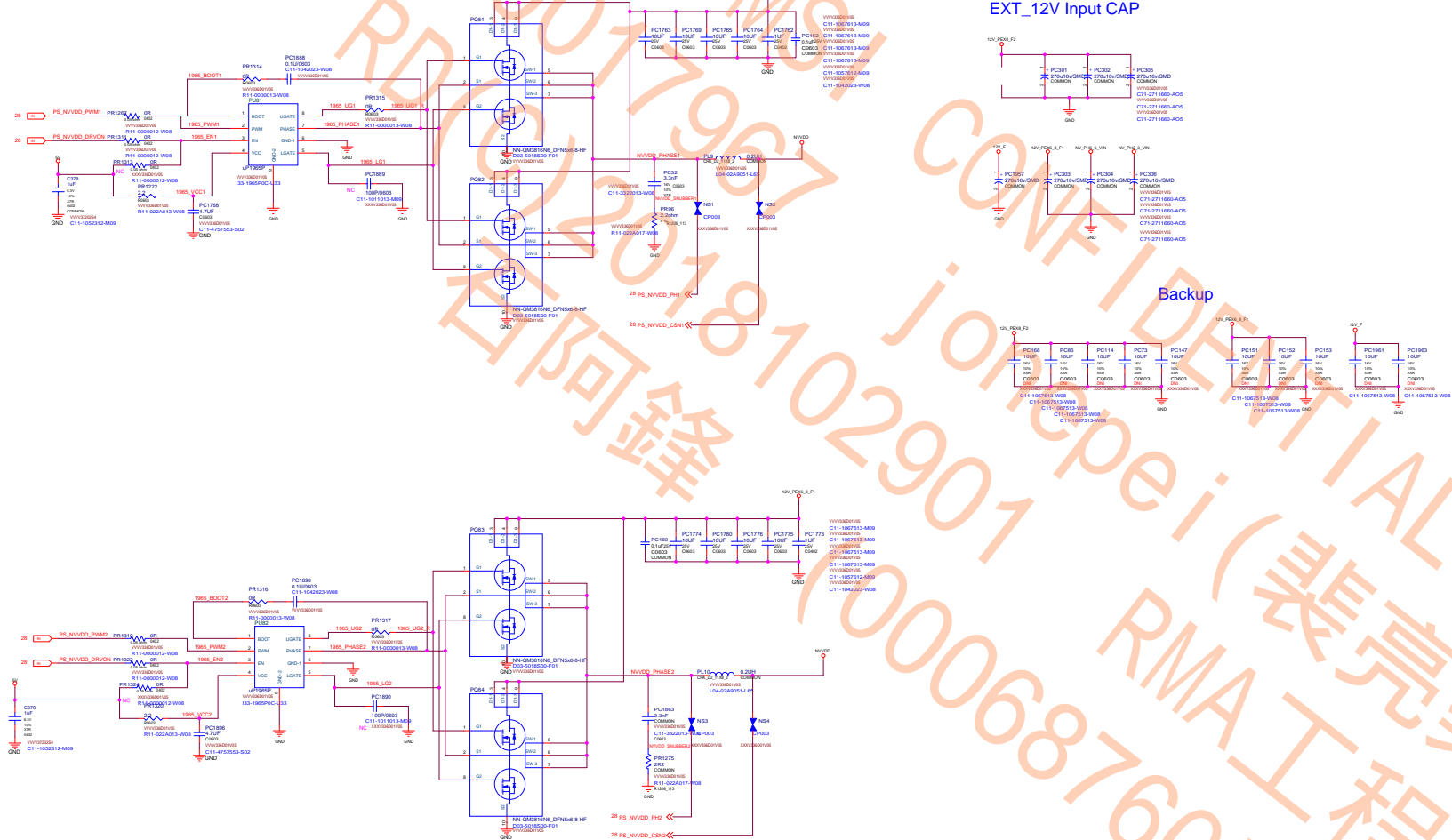


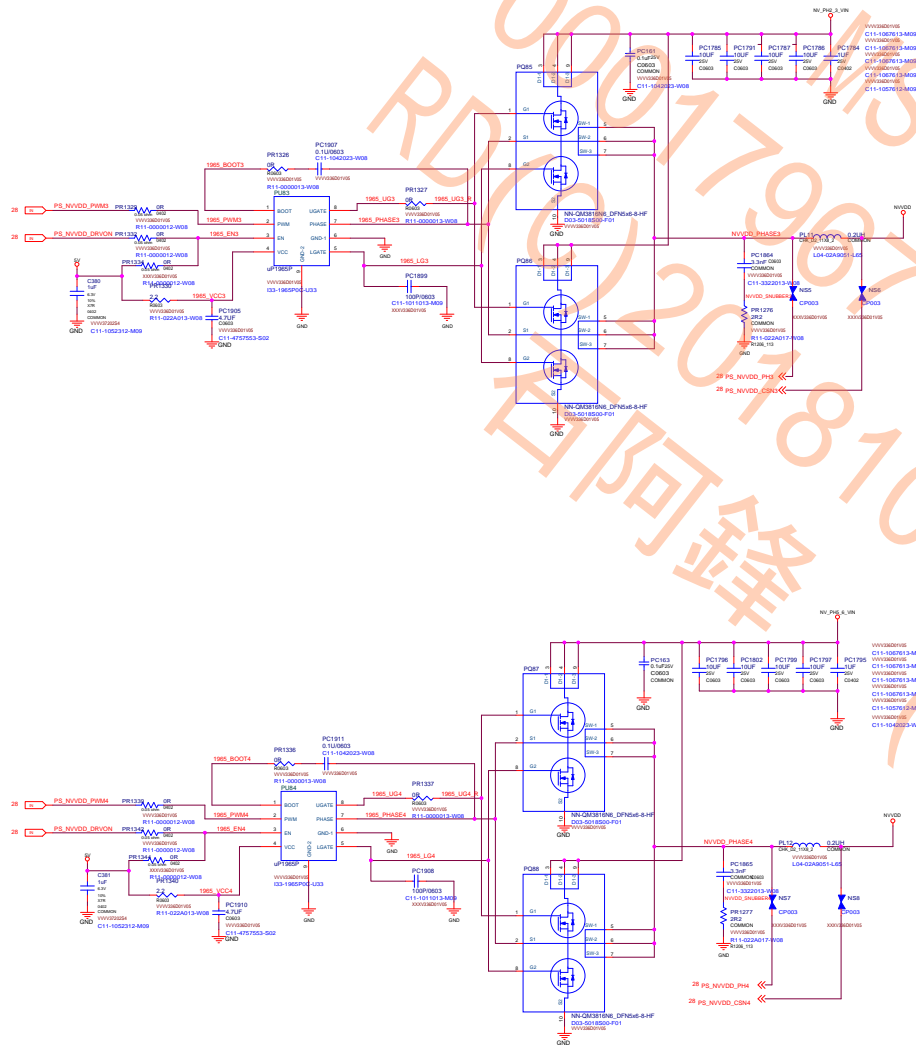


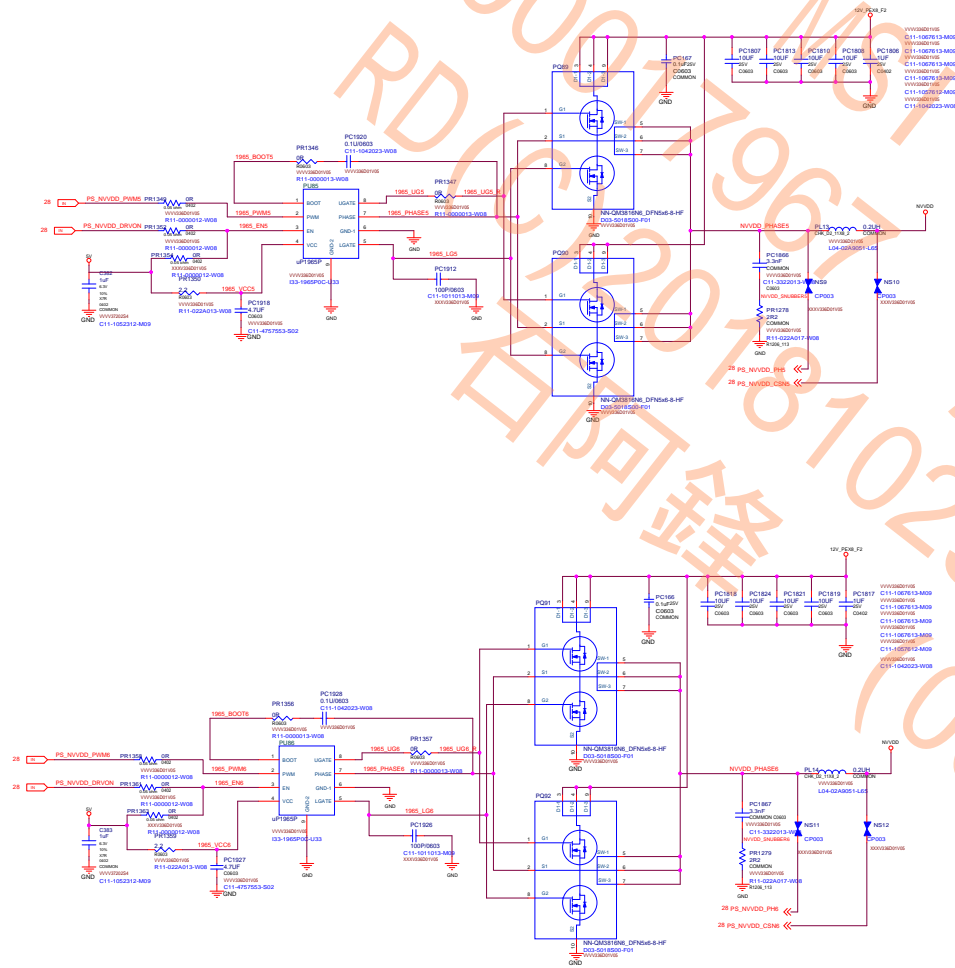
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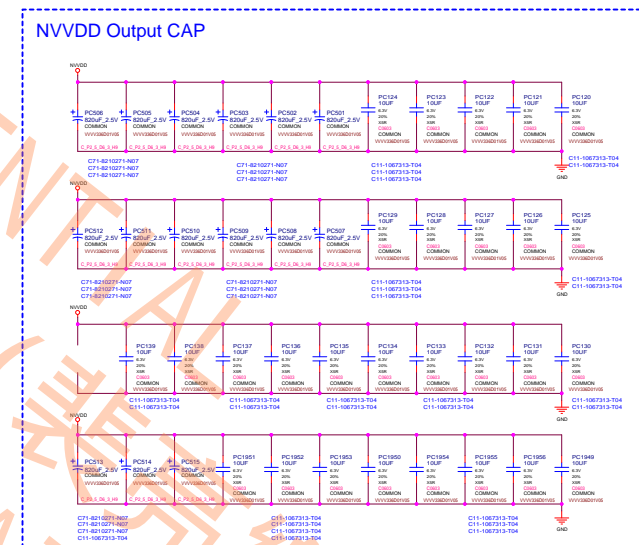
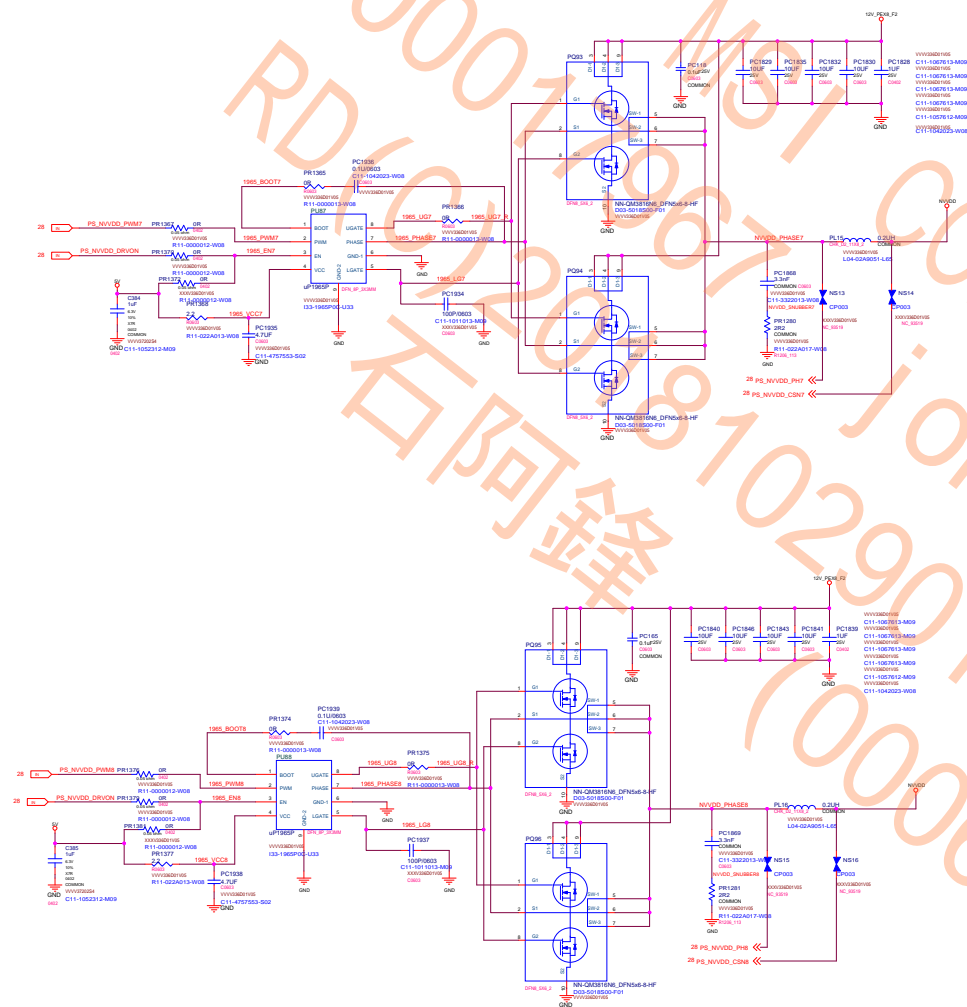
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MS-V373		
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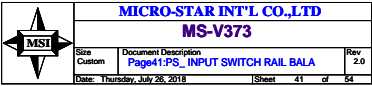




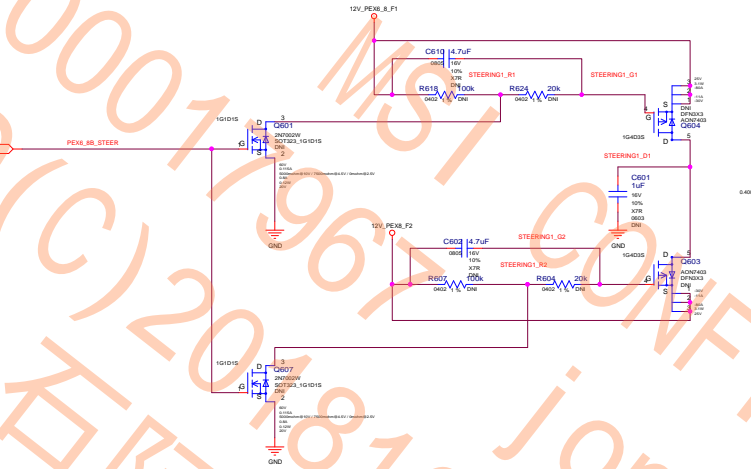




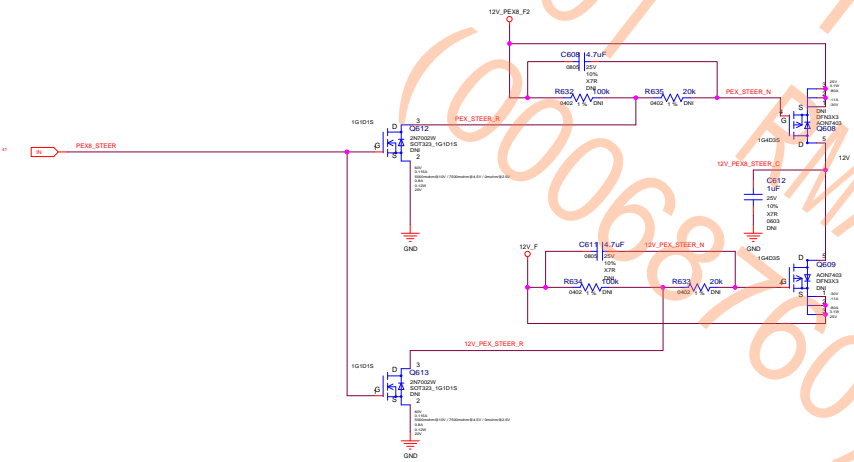




12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

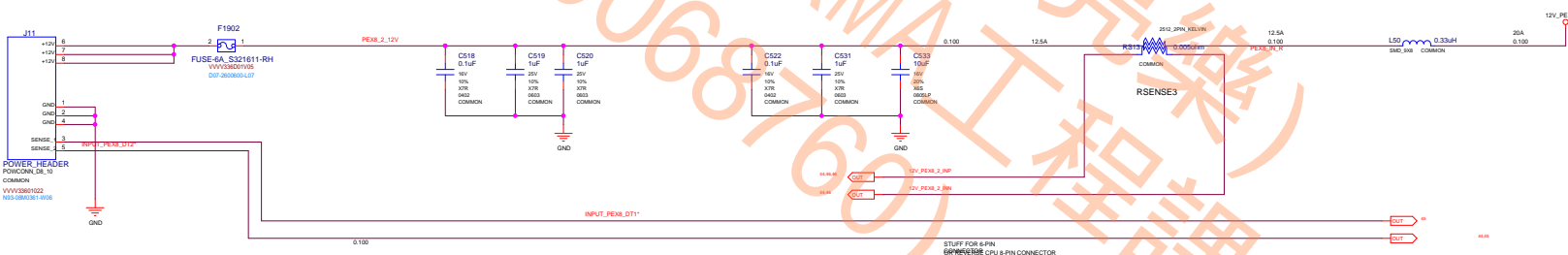
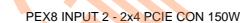
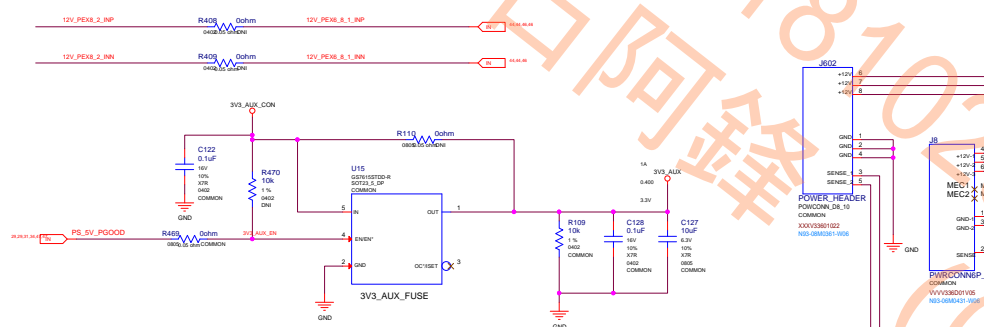
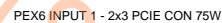
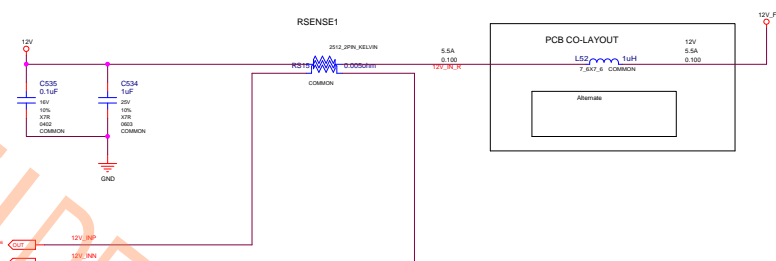
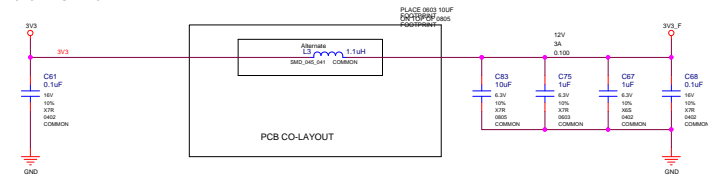
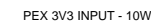
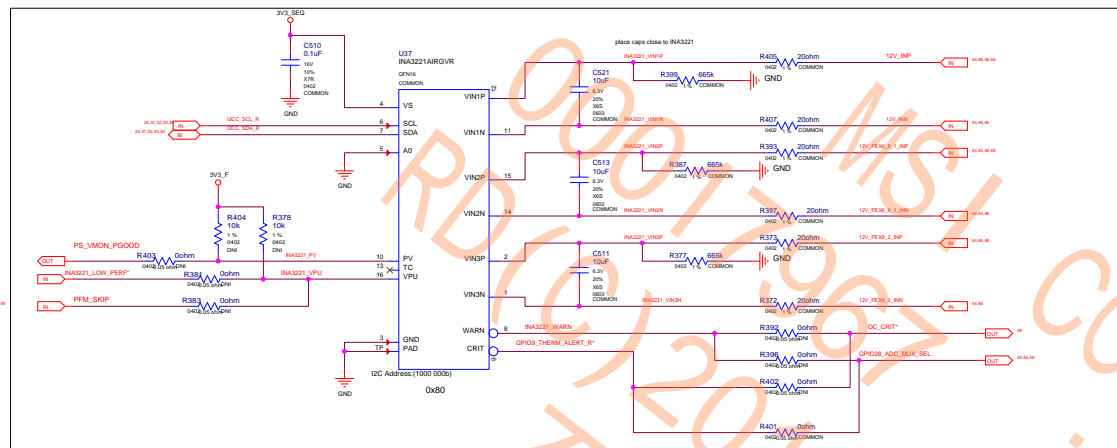


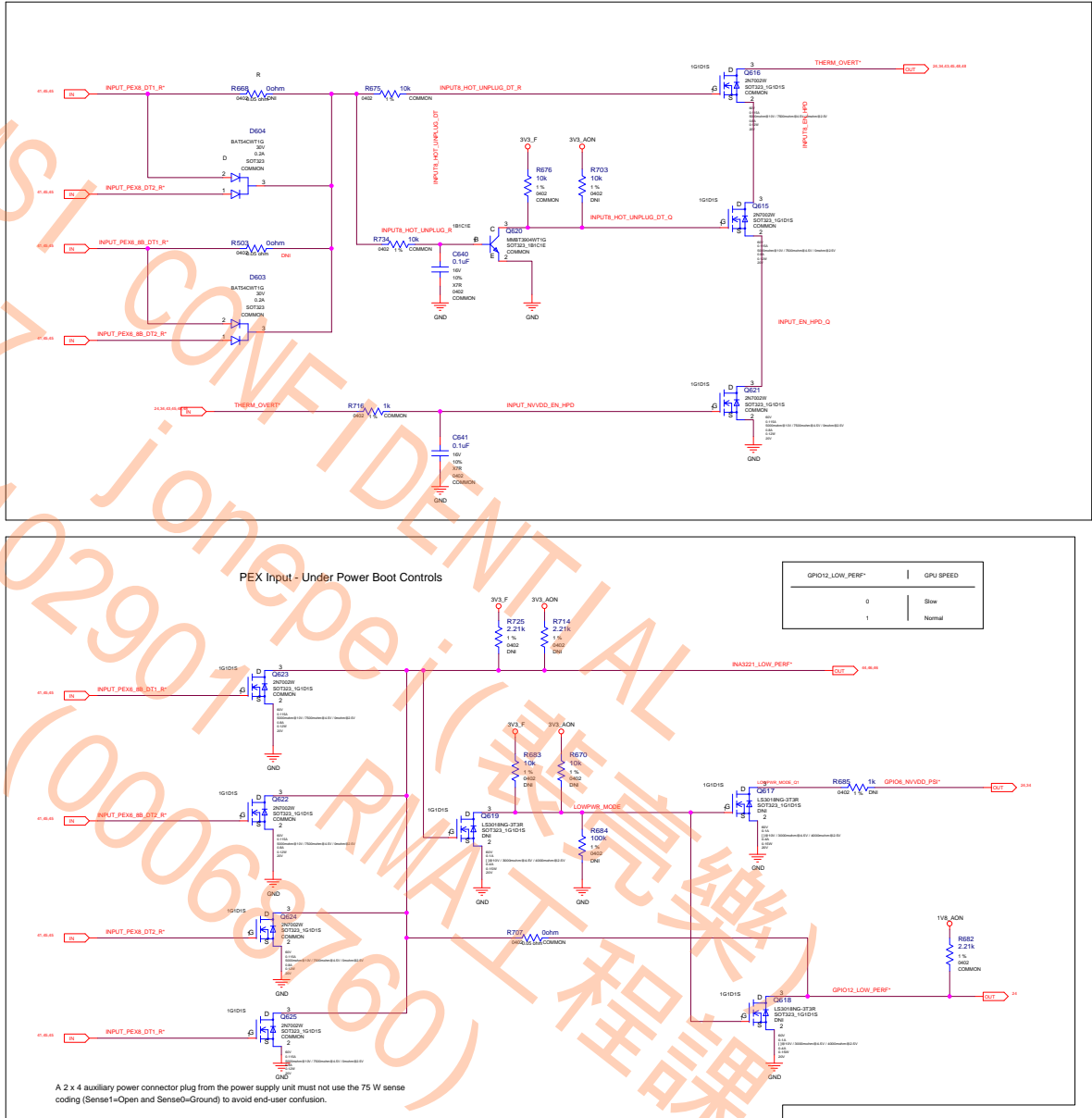
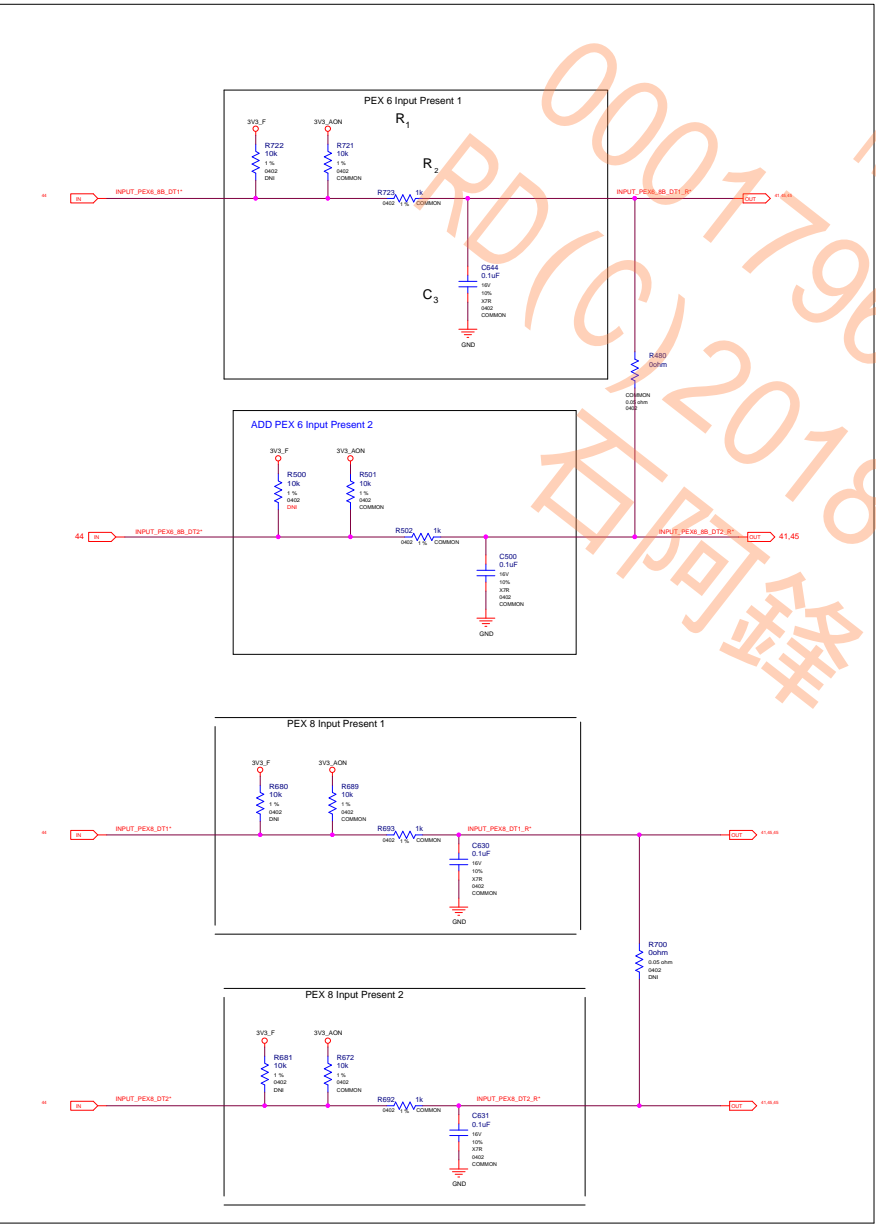
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

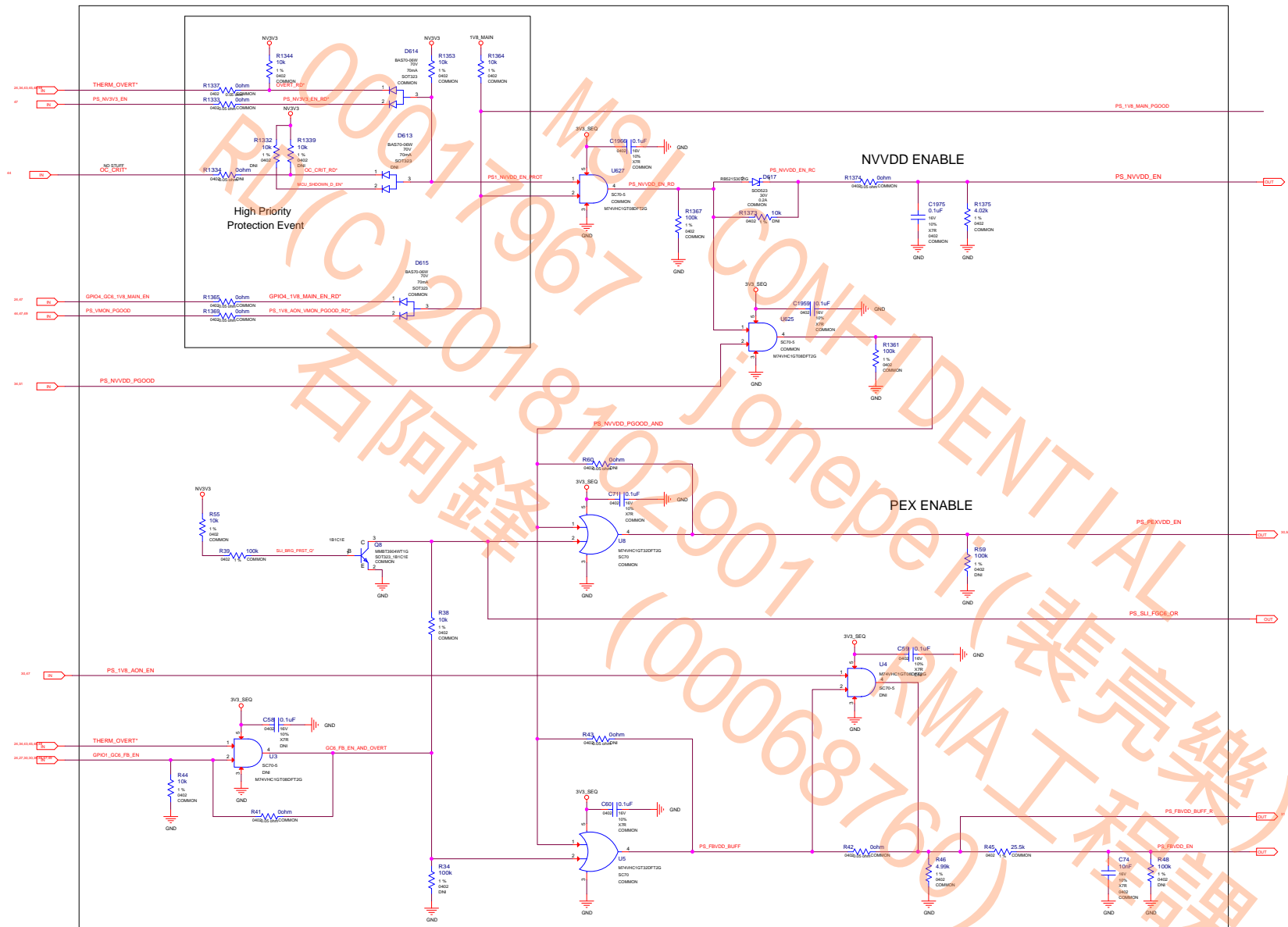


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石阿鋒 (00068760)

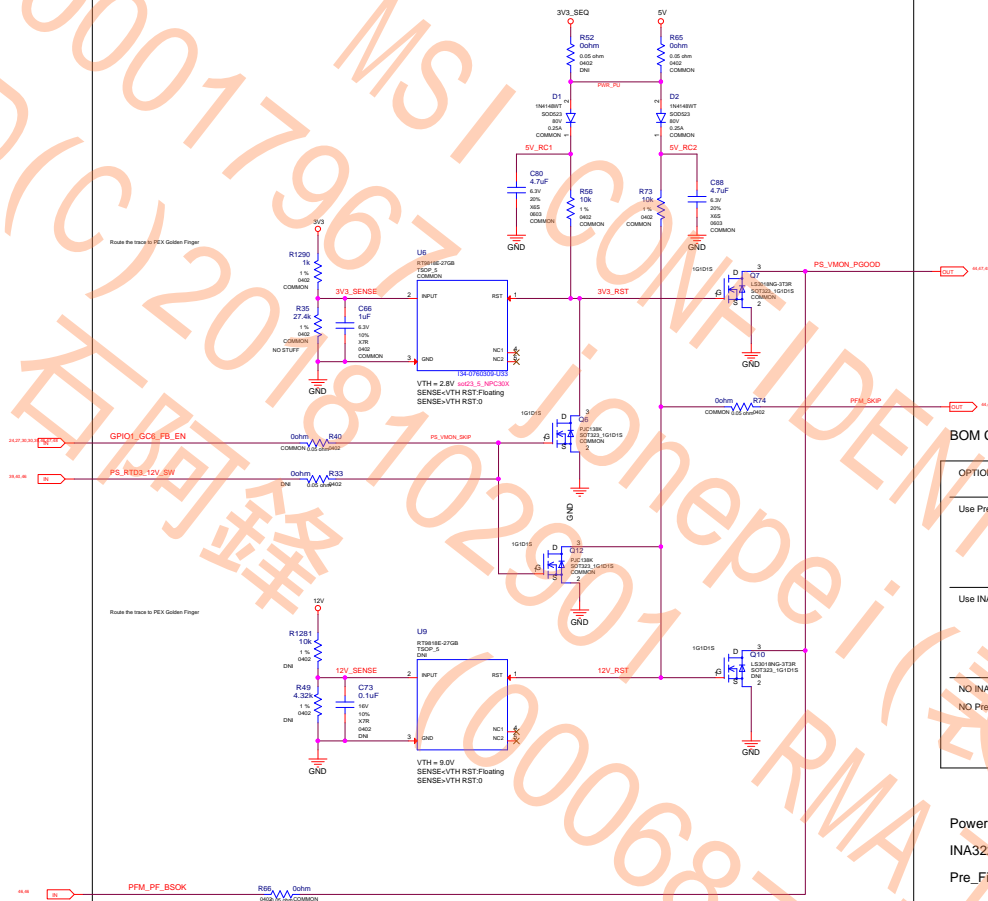
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PCIE Voltage Monitor



BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

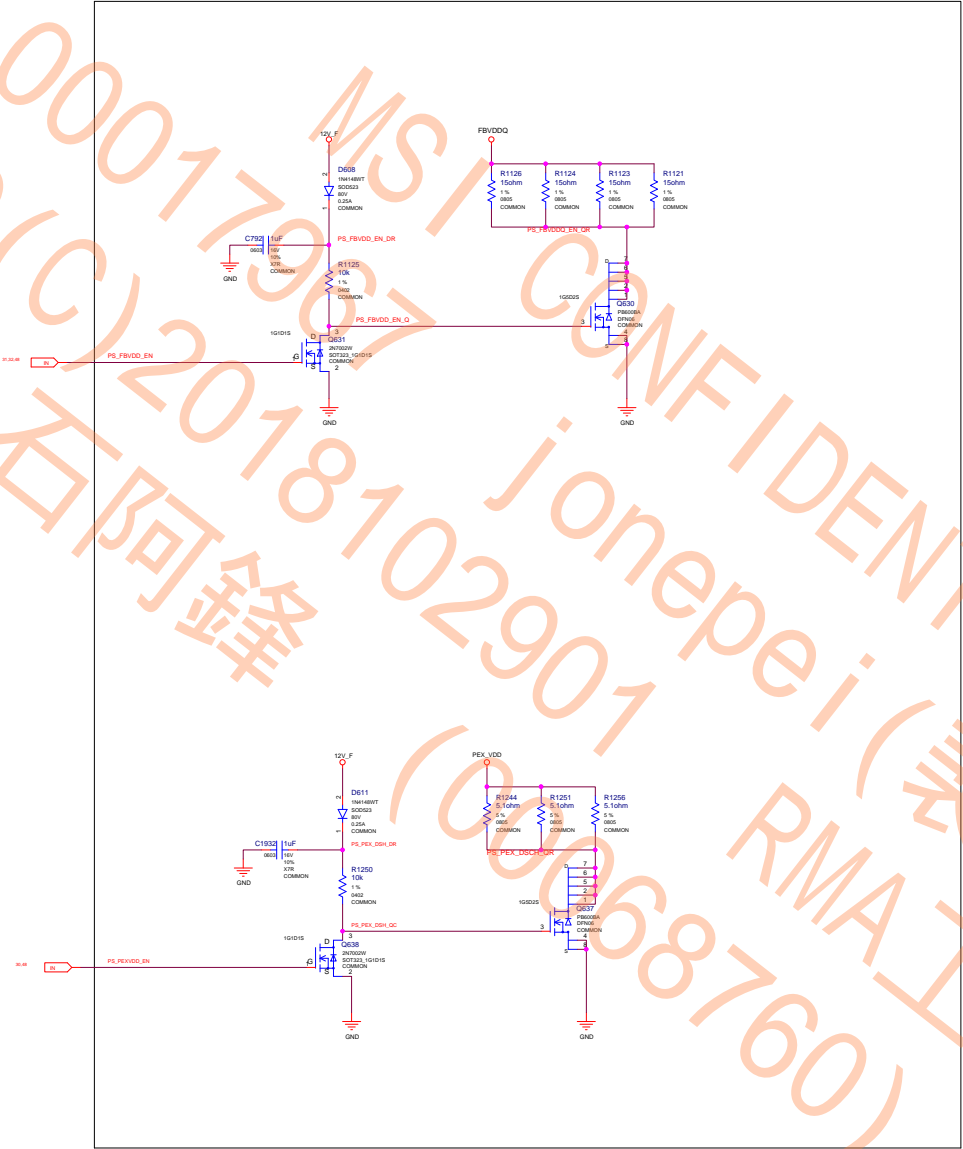
INA3221:3V3_SEQ

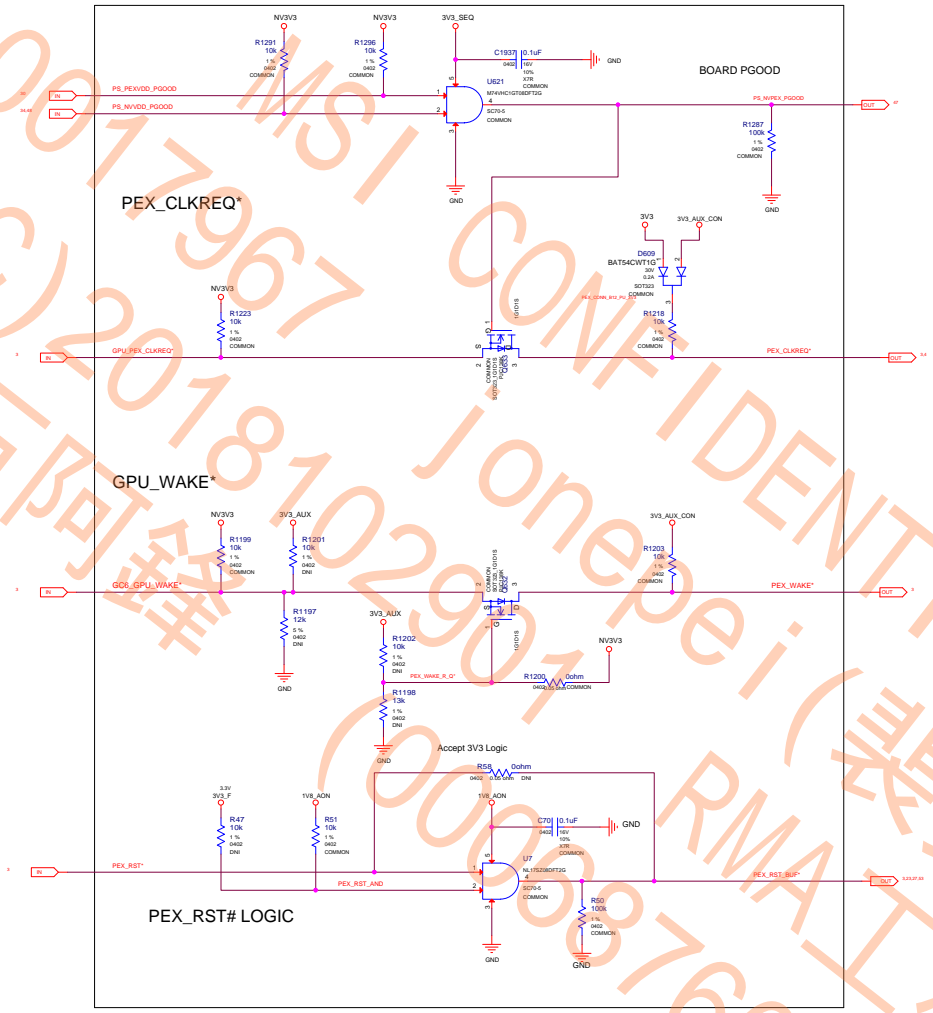
Pre_Filter(ADC_MUX):3V3(PEX)

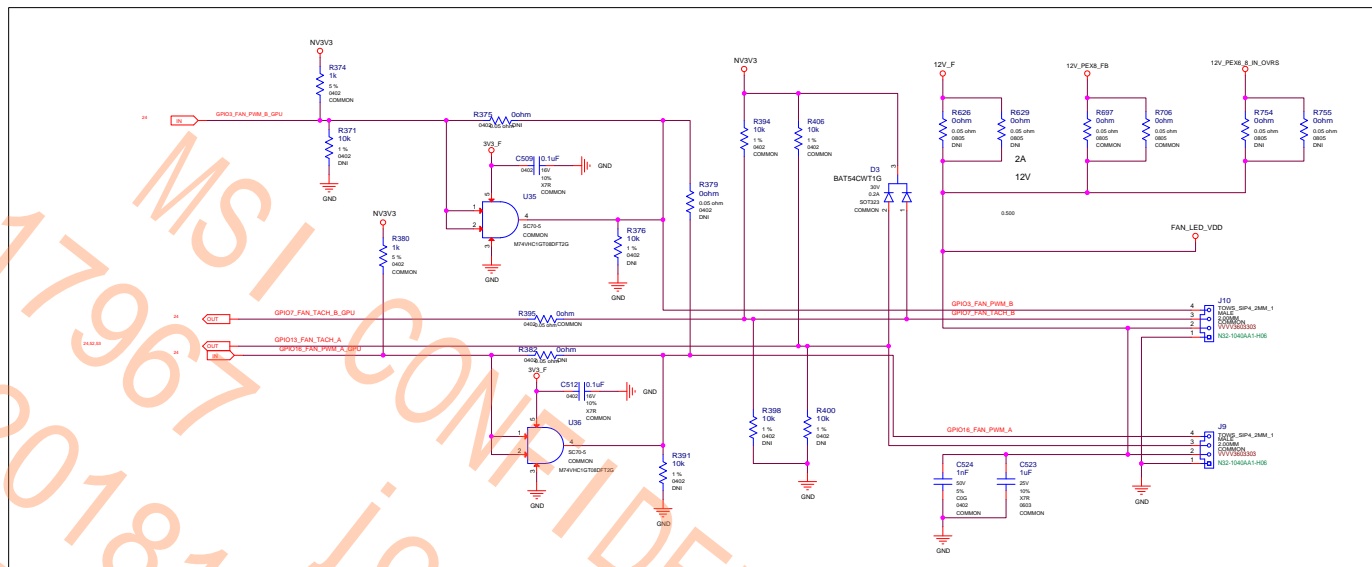
Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs


Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PG00D	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PG00D
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSK0	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW





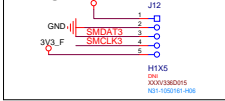
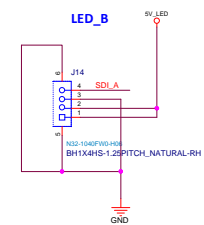
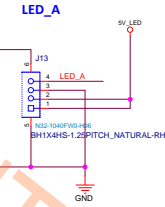
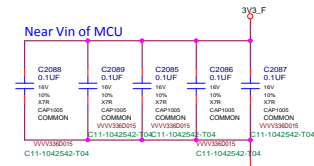
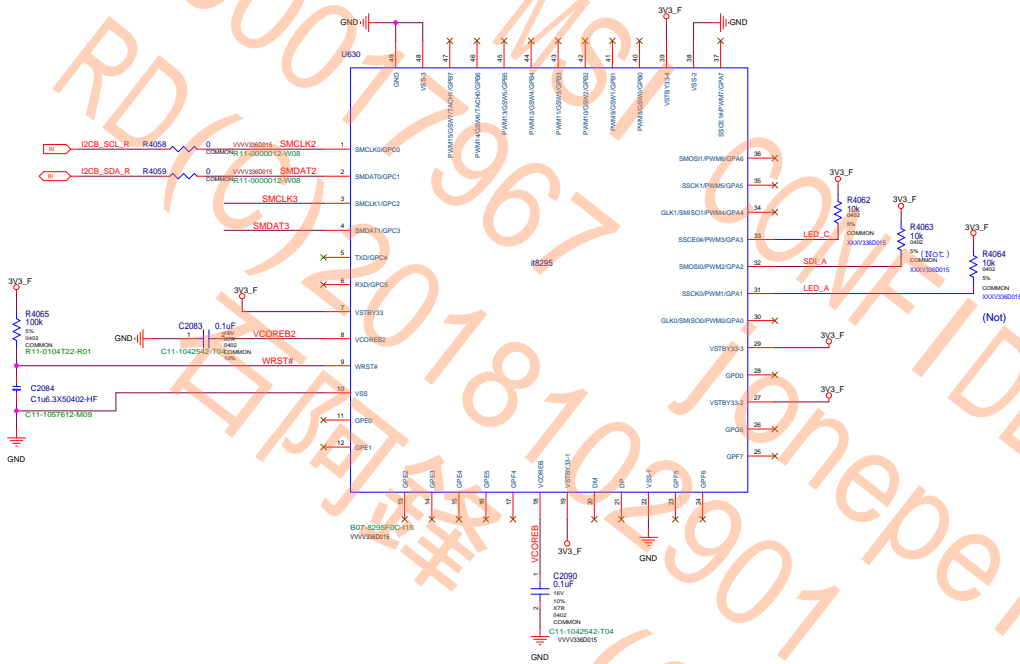
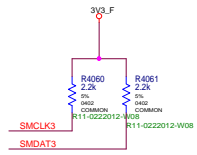


LED BOOST

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Firmware Programming

Debug

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5V_LED

